An Acoustic Charge Transport Imager for High Definition Television Applications

NASA Grant #NAGW-2753

W. D. Hunt and K. F. Brennan
School of Electrical Engineering
and
C. J. Summers
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

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Dr. William D. Hunt
Dr. Kevin F. Brennan
Dr. Christopher J. Summers

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School of Electrical Engineering and
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

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In this report we present the progress during the third six month period of the project. This includes both experimental and theoretical work on the acoustic charge transport (ACT) portion of the chip, the theoretical program modelling of the avalanche photodiode (APD) and the charge overflow transistor and the materials growth and fabrication part of the program. Among other results, we have the indication from a comprehensive experimental study that the use of a ZnO thin film piezoelectric overlay can reduce the RF power consumption of a typical ACT device from 28 dBm to 8dBm.

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An Acoustic Charge Transport Imager for High Definition Television Applications

W. D. Hunt, K. F. Brennan and C. J. Summers
Georgia Institute of Technology
Atlanta, Georgia 30332-0250

This report describes work performed during the third six month period of the ARPA/NASA sponsored project, "An acoustic charge transport imager for high definition television applications." This section presents a brief summary of those accomplishments. Our approach has been to work on the three components of the HDTV imager chip: the avalanche photodiode (APD) for image detection, the charge transfer device (CTD) for the collection and transfer of photogenerated charge and the acoustic charge transport (ACT) device for readout of the photogenerated charge. We anticipate the merger of some of these components during the next six month period. Herein we discuss our progress in each aspect of the HDTV imager chip.

We have completed the present series of experiments on the SAW properties of ZnO layers on GaAs substrates and have found that DC-Triode-sputtered ZnO layers provide enhanced piezoelectric coupling with relatively modest acoustic attenuation. We anticipate that the use of a ZnO layer will reduce the RF power required for acoustic charge transport by 20dB. This issue of excessive power consumption has been one of the primary complaints about ACT technology when it has been considered for commercial applications and this improvement would bring down the power requirements to about 8 dBm. Thus our findings have commercial implications for ACT device spinoffs in addition to the HDTV

imager. A portion of this work was presented at the 1992 IEEE Ultrasonics Symposium last October and a comprehensive paper is in preparation for journal publication. We collaborated with Motorola on this work and anticipate that they will soon join us as an industrial partner.

We initiated our study of the manufacturability of the HDTV imager chip and will present a conference paper at the 1993 IEEE International Electronics Manufacturing Technology Symposium. Through the inclusion of this sort of thinking we will be able to do yield modelling during these early phases of architecture development to ensure that our approach is a manufacturable one.

Work progressed on ACT device measurement and modelling with continued development of our physically-based small-signal circuit model for heterostructure ACT devices. In this we are simulating the frequency response and noise figure of ACT devices and our predictions agree within 1 dB of measured and published data. We investigated potential applications of ACT devices in mobile radio, specifically a "RAKE" receiver and presented the idea to Bell Northern Research (BNR). Pursuant to this we were able to sign BNR up as an industrial partner and they will be fabricating some ACT devices for us during the next reporting period.

Further improvements were made in our battery of engineering tools, in particular we wrote macros for use with the EESof Software program which allow us to lay out an ACT device mask in this RF simulation environment. Within a year we hope to have these macros fully incorporated into the environment so that we can go directly from device simulation to mask generation. Most of the foundation has been laid for the fabrication

processes associated with this program. This includes the ACT device and the charge transfer device. We are close to having these processes under control. Additional improvements were made in the characterization of APDs. There was also considerable effort put into the refinement of our MBE growth processes for larger scale, 2" , wafers.

More work was done on the design and optimization of a low-voltage avalanche photodiode for use in the imager array. Specifically we investigated the use of delta doping in the quantum well and barrier APD structures and found that significant improvement in device gain can be attained without much sacrifice in the noise of the device as long as some residual hole ionization is allowed to occur. The shortcoming of this design is that the gain can fluctuate significantly with variations in device parameters and operating bias. In the near future we will be investigating ways to resolve this shortcoming.

Extensive progress was made towards improving the accuracy of the computer simulations for studying the APDs. Specifically, we have developed a new approach to formulate the impact ionization transition rate which includes the k-dependence of the ionization rate. This will allow us to make a far better assessment of the optimal performance of the APD device.

An Acoustic Charge Transport Imager for High Definition Television Applications:

Third Semiannual Report

William D. Hunt and Kevin F. Brennan
School of Electrical Engineering
and
Christopher J. Summers
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332-0250

ABSTRACT

In this report we present the progress during the third six month period of the project. This includes both experimental and theoretical work on the acoustic charge transport (ACT) portion of the chip, the theoretical program modelling of the avalanche photodiode (APD) and the charge overflow transistor and the materials growth and fabrication part of the program. Among other results, we have the indication from a comprehensive experimental study that the use of a ZnO thin film piezoelectric overlay can reduce the RF power consumption of a typical ACT device from 28 dBm to 8 dBm.

1.0 Work Accomplished During This Period: ACT Program

Over the past six months work has progressed on several fronts. We have completed a series of acoustical experiments on ZnO on GaAs substrates which indicate that DC-Triode-sputtered ZnO layers provide enhanced piezoelectric coupling with relatively modest acoustic attenuation. Within the next few months we plan to fabricate ACT devices with ZnO thin film overlays and evaluate performance enhancements. We have enhanced our design for manufacturing capabilities by establishing mask design facilities within the EESof™ software program environment. This will allow us to go directly from our modelling of device performance to the semiconductor mask. Further, we have developed a physically based small-signal circuit model for ACT devices in the EESof™ environment which will allow us to model the noise, charge capacity and frequency response.

1.1 ACT Device Measurement and Modelling

1.1.1 A Physically-Based Small-Signal Circuit Model for Heterostructure ACT Devices

We have developed a small-signal circuit model for heterostructure acoustic charge transport (HACT) devices [1,2]. Circuit elements and noise sources are derived from operating conditions and physical device parameters. Frequency response and noise figure are simulated using EESof™. They agree within 1 dB of measured and published data.

The basic architecture of many ACT devices is that of a periodically tapped transversal filter, similar to those realized using digital signal processing (DSP) techniques. Being parallel analog processors, ACT devices offer a three-order of magnitude improvement in speed (bandwidth) over DSP-based transversal filters. Because of this, they have found applications as high-speed equalizers, programmable filters, and correlators.

Given these increasingly complex applications, computer modelling of ACT devices has become important not only to device designers, but also to systems designers who wish to predict overall performance based on device performance. In view of this, a device model must be detailed enough so that adequate information concerning device geometry and material parameters can be incorporated. It must also be flexible enough to provide tractable system level performance predictions. Previously reported models fall into two categories which address these needs individually. Computationally intensive Poisson-based physical models provide information about the charge density and potential within the device, but dynamic terminal characteristics are not easily obtained in this manner. Empirically based behavioral models provide adequate information for the system designer, but do not relate this to the internal operation of the device. We have developed a compromise between these two types with a physically-based small-signal circuit model. The element values of this model are derived from the device physics. Because it relies exclusively on linear time-invariant circuit elements, the equivalent circuit we report is easy to implement on commercially available microwave circuit analysis software.

Figure 1.1 shows the structure of the ACT devices tested. Three operations occur in the device: input sampling, charge transfer, and output sensing. Following this, the circuit model shown in Figure 1.2 is broken up into three sections. The development of the model allows noise sources, which appear in each of the three operations, to be linearly superimposed by mean-square superposition. The input structure is similar to a HEMT FET. Channel current is modulated by the depletion width variation, which in this case is dependent on both the gate and SAW potentials. Integrating the time-varying current over

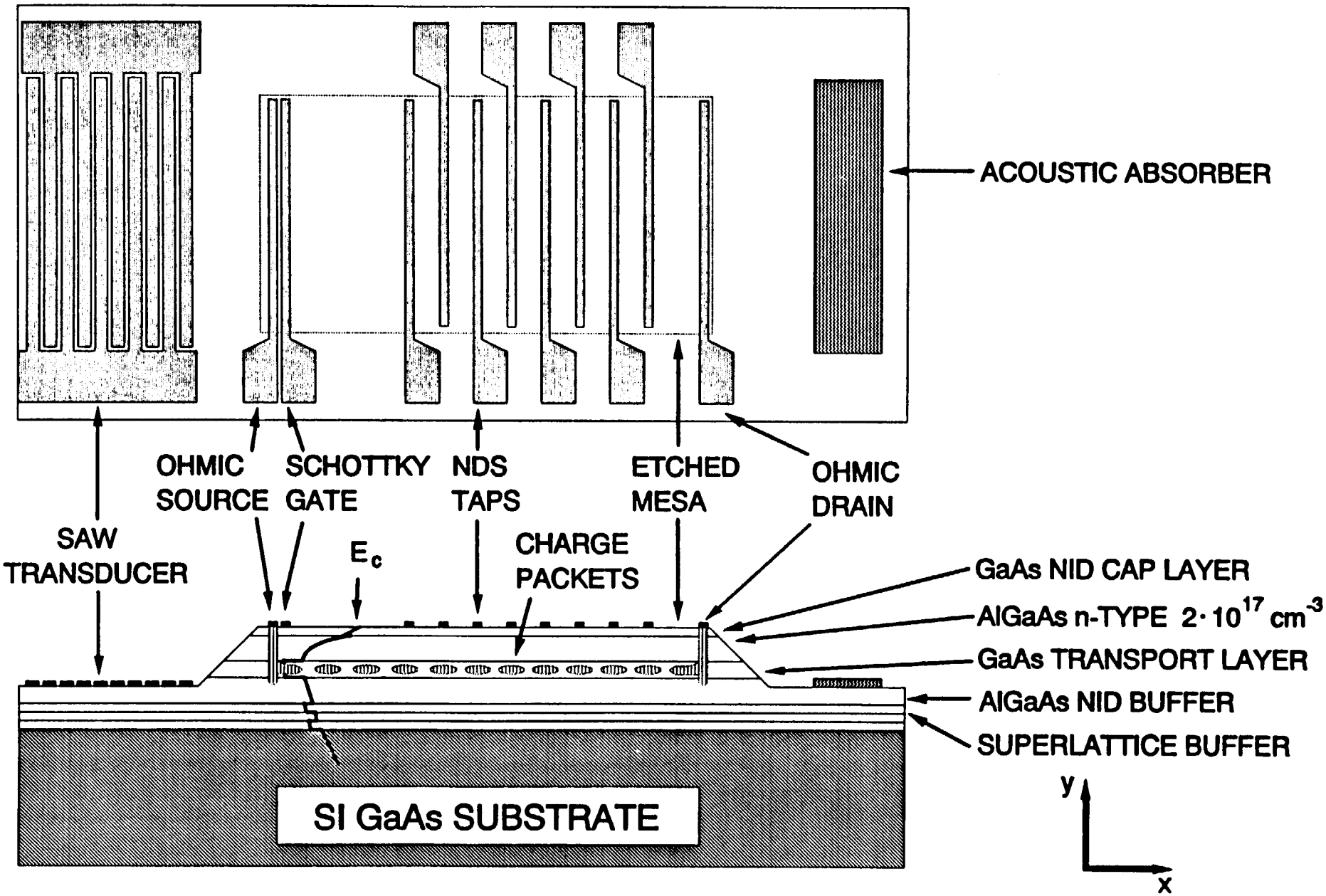


Figure 1.1 **Physical structure of a HACT device.**

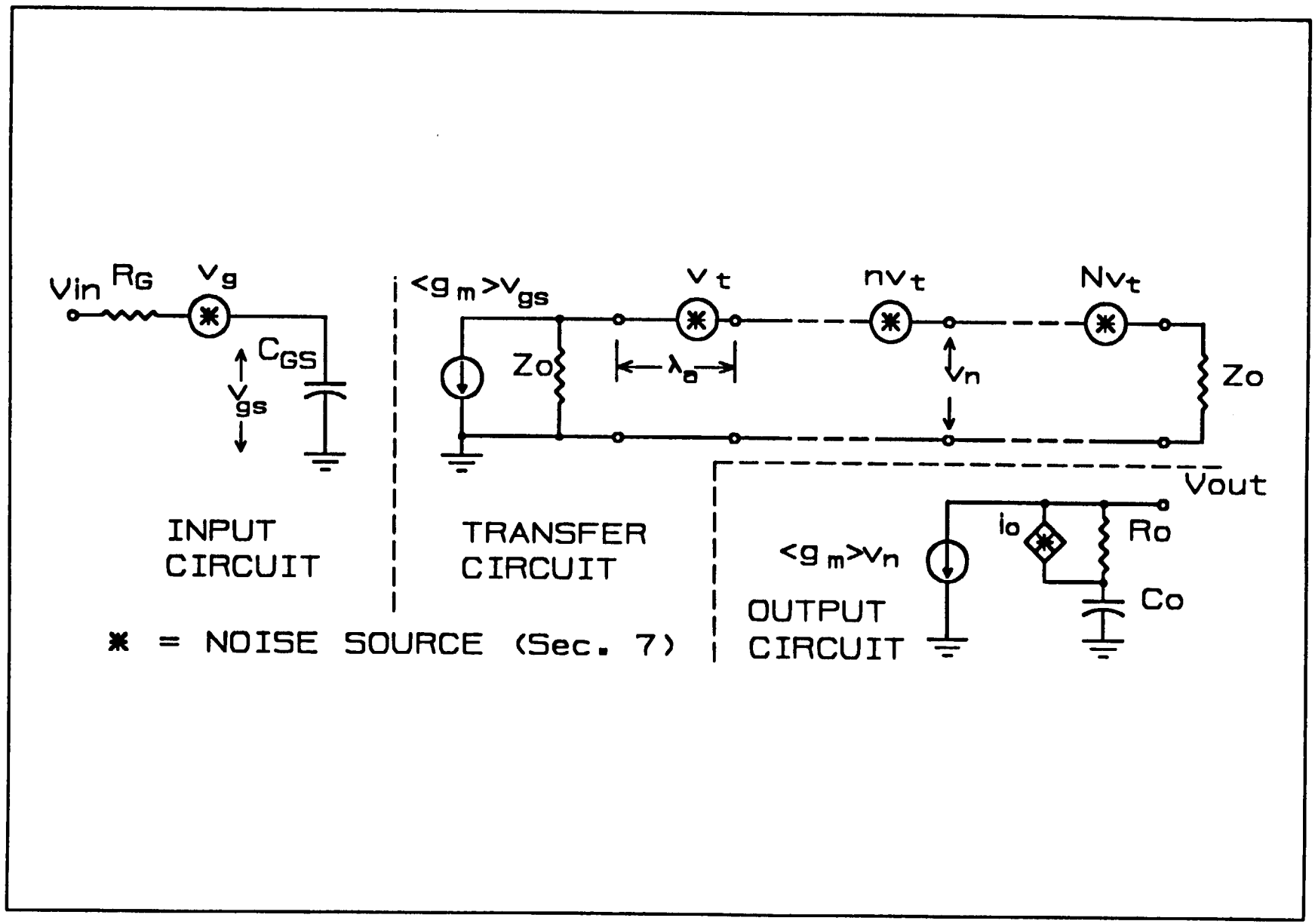


Figure 1.2 **Small-signal equivalent circuit for the HACT device.**

the clock period to obtain a "lumped charge" approximation, an expression for the steady-state small-signal transconductance is developed. For practical devices, this is quite low (50 - 300 μS) compared to a conventional HEMT FETs. This is because of the narrow sampling aperture, and the low doping in the channel required to keep from "shorting out" the SAW potential. The transfer operation is essentially a delay, and is represented by a transmission line section with the propagation velocity equal to the acoustic velocity. The charge packets are nondestructively sensed (NDS) by an induced image current flowing in Schottky metal electrodes on the surface of the channel. Because of the proximity of the charge packets, the image current is essentially equal to the channel current. In this way, each NDS tap is represented by a controlled current source, and associated parasitics. Using values calculated from physical models, the small signal-frequency response of a 160 tap ACT device is simulated using EESof™. This is shown in Figure 1.3, along with the measured frequency response. The error is less than 1 dB above -30 dB insertion loss. Below this, the measured data is corrupted by noise in the measurement system.

Noise is associated with each process in the ACT device. Thermal noise, present at the input due to gate resistance, can be quite high for several reasons. To keep from shorting out the electric field at the channel surface, the gate length must be small compared to the acoustic wavelength. For the same reason, the gate can only be accessed from the ends of the Schottky metal. The combined effect of these results in high gate resistance. For these reasons, the input thermal noise can dominate the noise performance of some ACT devices. The Schottky metal structure that is used for the gate is also used for the NDS taps, and the same thermal noise is present here also. But this is essentially a second-stage effect,

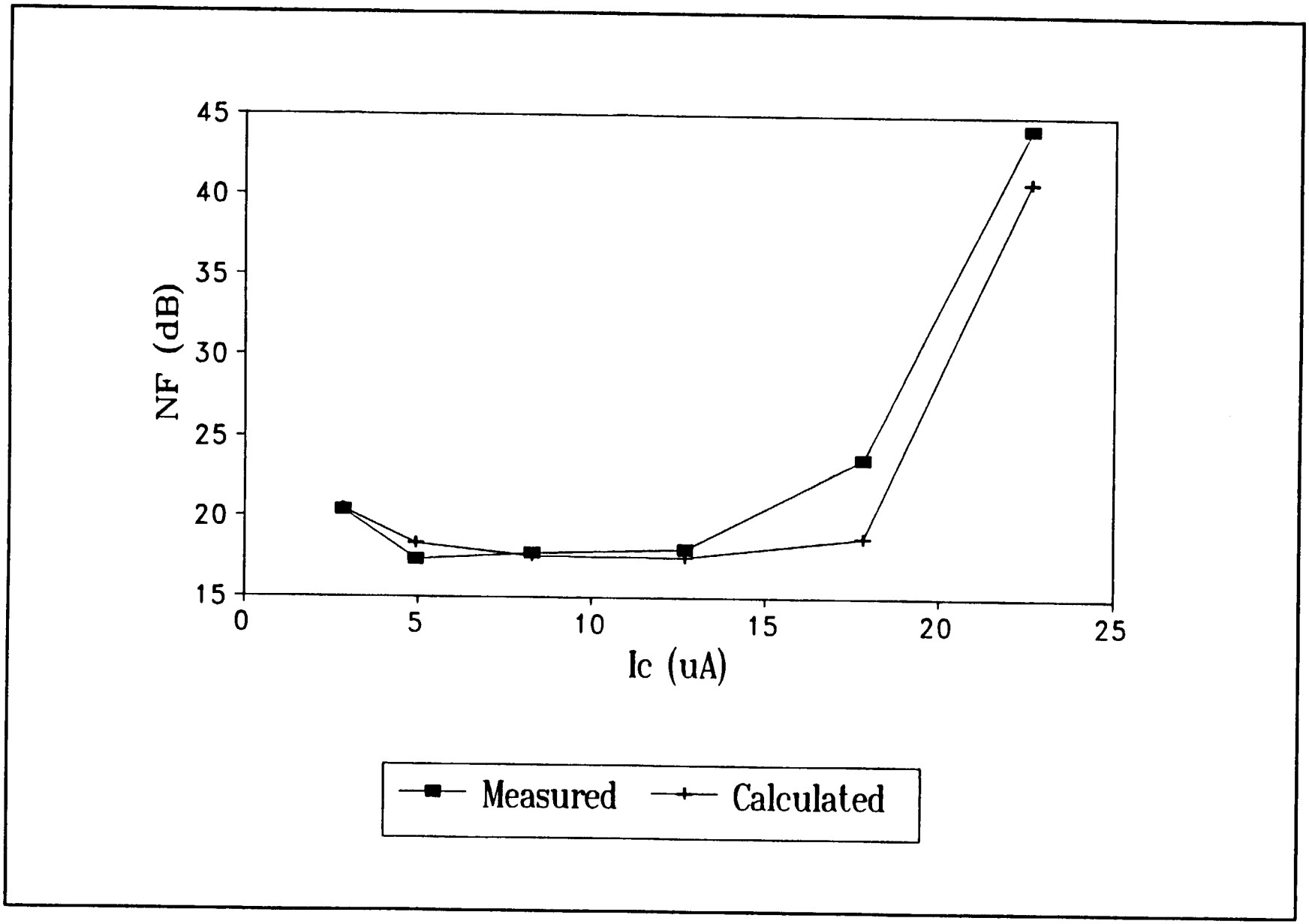


Figure 1.3 **Measured and calculated noise figure for a 160 tap HACT device vs. channel current.**

and is only significant for low transconductance devices. For ACT devices with long delays ($> 1\ \mu s$), *transfer noise* can become significant. It is caused by random trapping and emission of carriers in bulk and interface state traps. Expressions for the input, output, and transfer noise are developed. The thermal noise sources are inherent in the resistor models used in EESof™. The transfer noise is represented by an equivalent noise voltage source at the transfer circuit input. The simulated and measured noise figure at band center of a 160 tap HACT is shown in Figure 1.4. Better than 1 dB agreement (about 5% error) is obtained below the channel saturation current ($\approx 15\ \mu A$). Above this, the model is invalid because of charge diffusion.

1.1.2 Potential Applications of ACT Devices in Mobile Radio

Due to our close association with Bell-Northern Research, we have investigated the potential applications of ACT devices in mobile radio systems and made a related presentation to their technical staff.

We discussed the advantages of ACT technology over conventional DSP technology to implement real-time transversal filters. A short description of the physics of ACT device operation were given. The mobile radio propagation environment was then discussed, with emphasis on wideband channels. Equalization architectures were presented that are used to alleviate the effects of frequency selective multipath fading. One such architecture has been called the "RAKE" receiver, which is essentially a transversal filter bank that sorts the received, delayed replicas of the transmitted signal, and recombines them in such a fashion as to minimize the signal-to-noise ratio at the detector. To illustrate the utility of technology in implementing RAKE receivers monolithically, we discussed a design example of a T-1

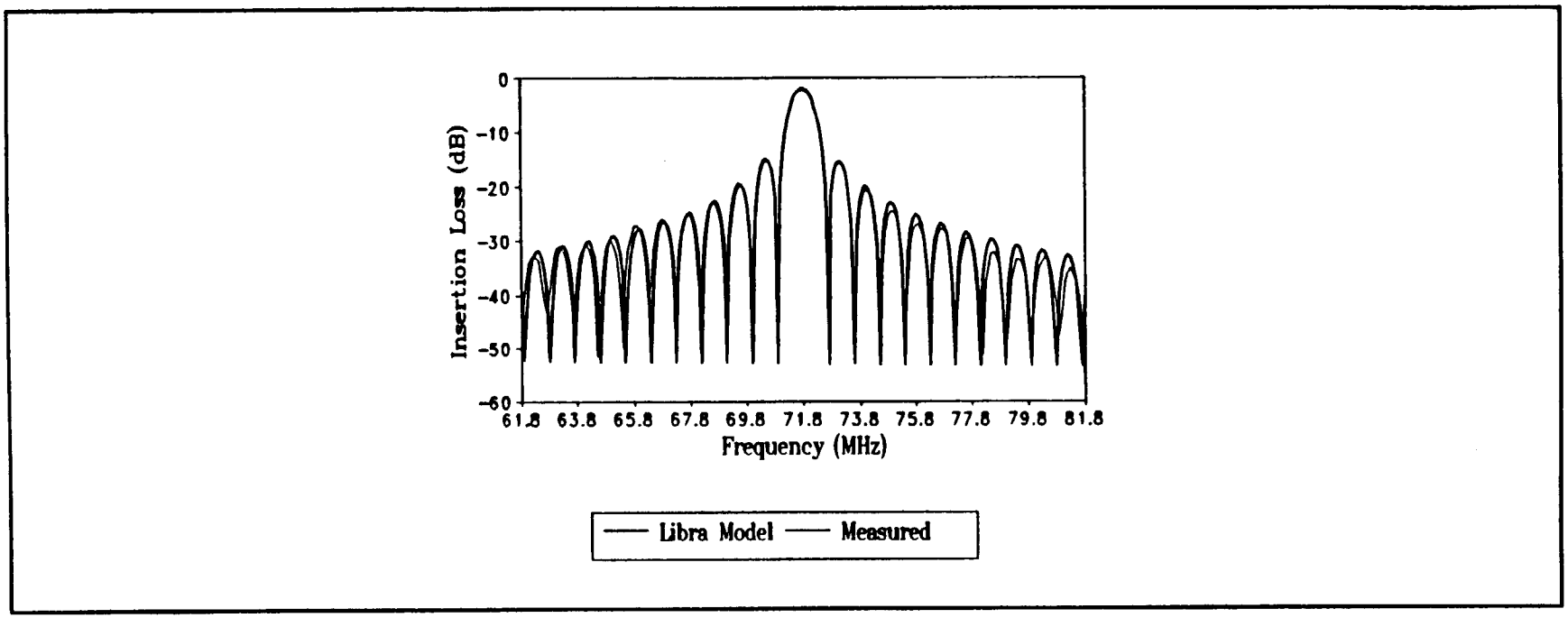


Figure 1.4 Measured and simulated small-signal gain of a 160 tap HACT device.

(1.544 Mbit/sec) rate wireless LAN applications. This example highlighted the high computational abilities of the ACT device in that the wireless local area network (WLAN) RAKE receiver required in excess of 25 billion multiply and accumulate instructions per second to give the equivalent performance of a 4-diversity receiving system. This is roughly three orders of magnitude faster than the current state of the art in DSP processors.

1.1.3 ACT Process Modelling

In cooperation with Professor Gary S. May of the School of Electrical Engineering at Georgia Tech we have begun to investigate process yield modelling for ACT devices and the HDTV camera [3]. We anticipate that we will have a conference paper and a journal paper on this later this year. This work will aid us tremendously in the design and high yield fabrication of the HDTV camera chip.

1.2 ACT Device Design and Fabrication

Over the course of the past fifteen months, several groundbreaking phases of work on the HDTV Project have been completed. These phases include the development of the ACT prototype mask set, an electrical characterization mask set, a cleanroom fabrication process traveller, and the testing and calibration of cleanroom equipment. This work has enabled our group to begin realizing prototype ACT devices for their acoustical and electrical characterization. As data is presently being collected from these devices, theoretical work is being performed to help more accurately model the ACT device from an acoustical standpoint using the Coupling of Modes (COM) Method; furthermore, another acoustical characterization mask set is being generated to investigate alternate substrates for the ACT device. In this report, a brief summary shall be given of the work completed earlier this

year and a description of current research will be presented.

Last year, several major steps which has lead to the fabrication of prototype ACT devices have been completed. The first step was the design and layout of an electrical test characterization mask set illustrated in Figure 1.5. This electrical test cell was designed to allow the characterization of several electrical parameters of ACT substrates and contact metals: Hall carrier mobility, sheet and contact resistance, electrical transconductance, photoinjection of carriers, etc.

This electrical test cell was later added as a die site in the ACT prototype mask set, its second revision illustrated in Figure 1.6. This five-layer mask set consists of sixteen (16) dies, two (2) electrical characterization cells and fourteen (14) prototype ACT devices. There are four different variations of the ACT prototype devices. Acoustically, each ACT device was identical using split-finger interdigitated transducers (IDT's) operating at a center frequency of 180MHz to provide a surface acoustic wave (SAW) to transfer the injected charges through the mesa region of the each ACT device. Each of the four variations of the ACT devices differed in the layout of the non-destructive sensing (NDS) taps placed over the mesa channel region to detect and measure the presence of acoustic charge transport.

As the ACT prototype mask set was being designed, a great deal of preparation went into the development of a cleanroom process traveller. An excerpt of this traveller can be seen in Figure 1.7. With this traveller, a precise record of fabrication steps could be detailed and checked-off as a ACT device was being processed in the Microelectronics Research Center (MiRC) Class 10 Cleanroom. Cleanroom experiments utilizing mechanical-grade gallium arsenide (GaAs) substrate wafers were performed to fine tune the traveller's

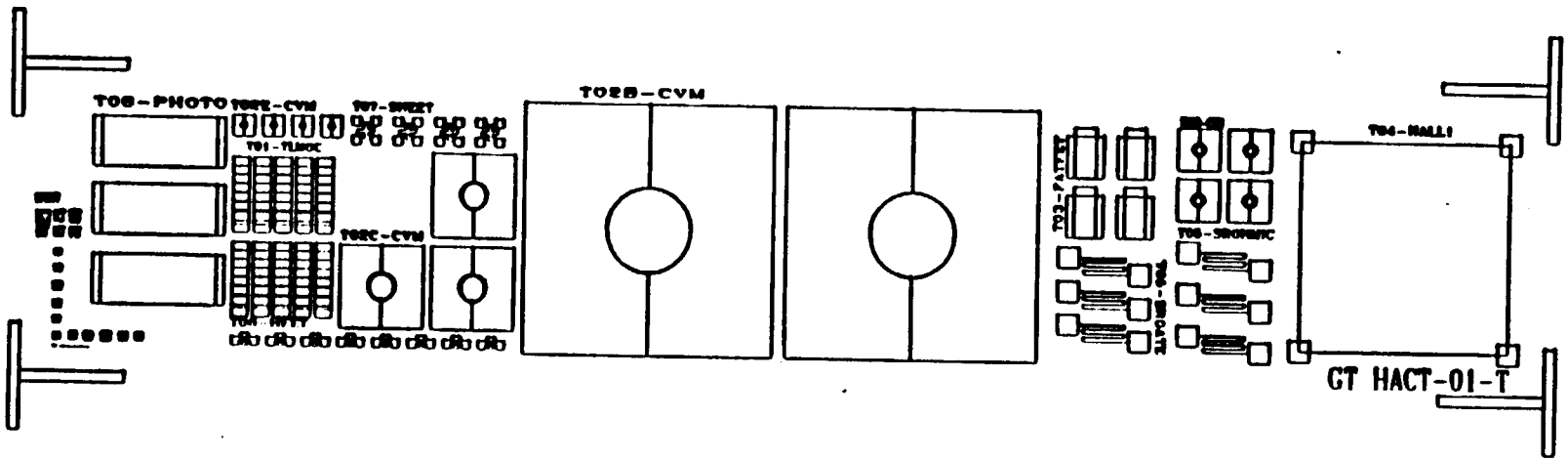


Figure 1.5 Electrical characterization test cell. (all mask layers)

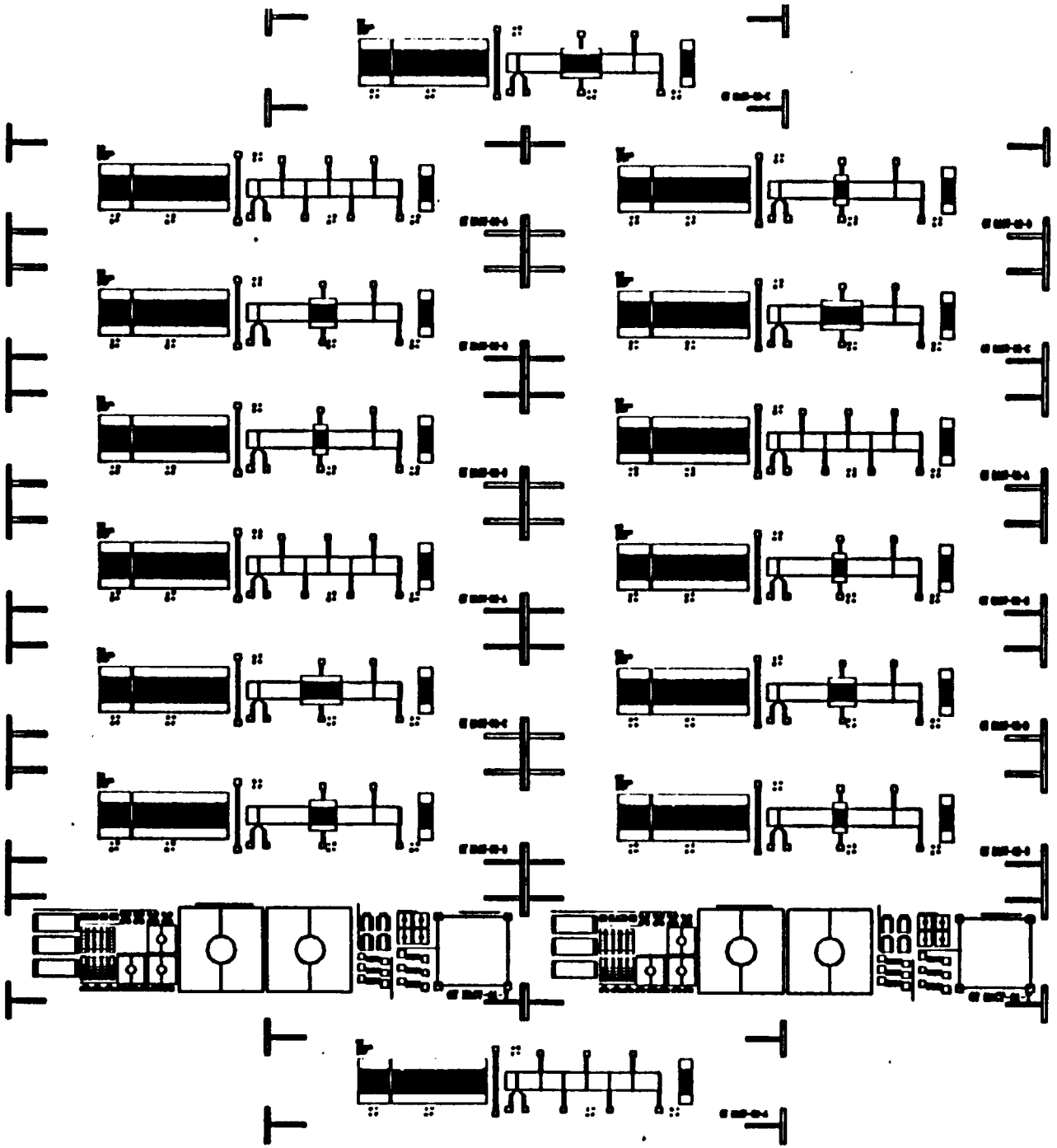


Figure 1.6 HACT prototype mask set, rev. 2. (all mask layers)

Manufacturing Traveler	
Project: HDTV	Date Started: 1/3/92
Job Number: EE 61-387	Date Completed:
MT No.: 100	Responsible Engr.:
Mask Set: HACT-01	Wafer Nos.:
Part Nos.: HACT-01A,HACT-01B,HACT-01C,	
HACT-01D,ELTEST.	
Part Description: 180MHz Tap delay line, 1λ memory array,3λ memory array, 3λ memory array, Electrical test cell.	Total Qty.:

STEP	OPERATION	DESCRIPTION	QTY	INT	DATE	REV
	Lot Initiation					
0.1	Kit wafers	Include one monitor wafer.				
0.2	Wafer Identification	Scribe wafer nos. on backside.				
0.3	Inspect wafers	Microscope inspection : Light field 5X, 20X, 50X.				
	Mesa Isolation					
1.0	Clean wafer	soak : spray TCE 1min : 15 sec Methanol 1min : 15 sec Acetone 1min : 15 sec Micro with swab Isopropyl 1min : 15 sec DI rinse 1min : 15 sec N_2 Blow dry				
2.0	Workmanship verification	Microscope inspection : Light field 5X, 20X, 50X.				
3.0	Dehydration bake	100°C for 30 min.				
3.1	Air cool	10-15 min.				
4.0	PR coat with AZ4330	spread: 1000 RPM for 2 sec. spin: 4000 RPM for 30 sec.				
4.1	Remove edge bead	Acetone with Q-tip. N_2 Blow dry.				
5.0	Pre-exposure bake	95°C for 30 min.				

COMMENTS

Figure 1.7 Excerpt of HDTV cleanroom process traveller.

fabrication steps, such as initial substrate surface preparation, photolithographic exposure and development processes, e-beam evaporator contact metal deposition, and ohmic contact annealing. Cleanroom experiments are still being conducted to further develop the process traveller to increase the fabrication yield of the ACT devices.

At present, their are two research areas being pursued to further progress the HDTV project. The current thrust is the design and layout of a generic acoustical characterization mask set, the first prototype illustrated in Figure 1.8. This mask will allow the fabrication of several different acoustical test devices on a substrate in order to measure fundamental acoustical parameters such as the electro-mechanical coupling coefficient (K^2), SAW velocity (v_{SAW}), and SAW propagation attenuation (a) as a function of frequency . Furthermore, certain specific SAW device parameters can be measured, such as the magnitude and phase of the reflection coefficient of a metal strip on the substrate, the optimum IDT-to-acoustical reflector spacing, and the first and second order mechanical and piezoelectric scattering coefficients of certain metals on the substrate. Through the use of a knife-edge laser probe system to make the acoustical measurements of the characterization devices to be constructed with this mask set, a variety of substrates will be acoustically analyzed in order to optimize the efficiency of the ACT devices. With the completion of this mask layout in April, the acoustical characterization of multi-layer indium phosphide (InP) and indium gallium arsenide phosphide (InGaAsP) substrates is being planned for June this year.

A second research pursuit involving the electro-mechanical modeling of the ACT devices is also underway. The modeling method being researched was first developed by Cross and Schmidt in 1977 and is entitled the Coupling-of-Modes (COM) Method. With this

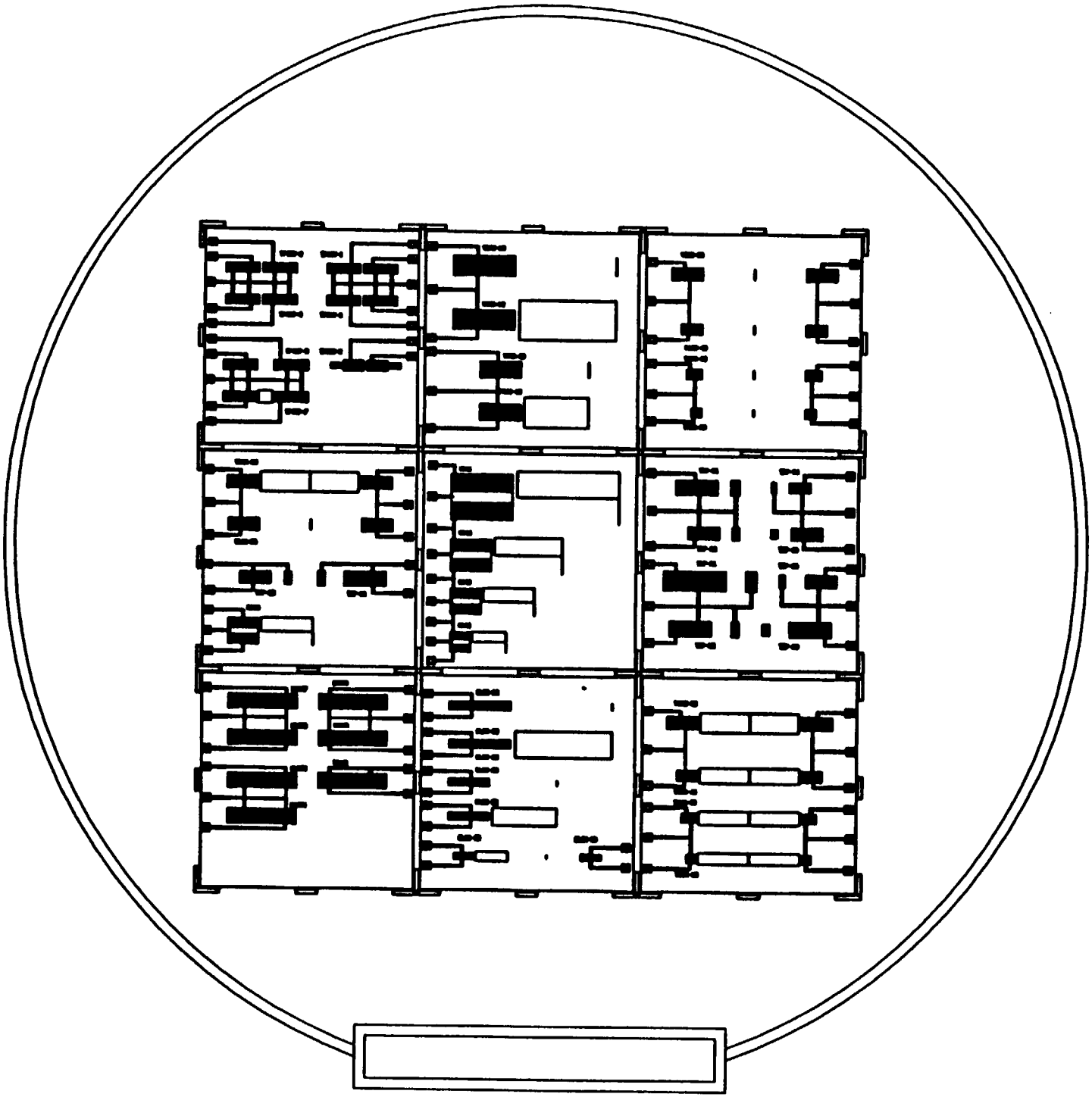


Figure 1.8 **Acoustical characterization test mask.**

method, virtually any variety of SAW devices can be modeled both acoustically and electrically using a hybrid acousto-electrical scattering parameter matrix for each IDT, reflective grating, and spacing element in a SAW device. By using packaged analysis software such as Mathematica and MatLab, or Lahey Fortran, the overall theoretical acoustical and electrical response of a SAW device can be obtained using simple linear algebra manipulations of the scattering parameter matrices and a variety of acoustical and electrical boundary conditions. Presently, experimental results from existing SAW and ACT devices are being used to compare results with COM simulations. With the fabrication of test structures from the upcoming acoustical characterization mask, it is hoped that experimentally obtained SAW substrate parameters and the output of further test devices can help fine tune the COM simulations to yield accurate acousto-electrical modeling of the ACT devices.

1.3 SAW Properties of ZnO Films on GaAs Substrates

Measured SAW properties of 1.6-4μm thicknesses of ZnO film over semi-insulating {100}-cut <110>-propagating GaAs substrates are presented, including velocity, K^2, attenuation for the frequency range of 180-360MHz. The diffraction associated with propagating SAW is also analyzed. Velocity surfaces are obtained using an angular spectrum of plane wave (ASPW) theory [4] since the geometry of anisotropic wave diffraction is well understood in terms of the velocity surface (or slowness surface). Laser-probed beam profiles on metalized and free surface of the filmed substrate are compared.

For the application of ACT devices, a passivation layer such as SiO_2 [5], Si_3N_4 [6], or SiON [7] might be required in order to: 1) passivate the structure and enhance the yield, 2)

prevent unnecessary doping of GaAs during subsequent fabrication processes. The application of such passivation layer was also considered in this experiment with a PECVD grown SiO_2 or CVD grown Si_3N_4 layer. The results with and without the passivation layer are compared with theoretical values.

C-axis oriented polycrystalline ZnO films have been grown using both rf and dc triode sputtering method on {100} cut GaAs wafer provided by LEC crystal growth.As a passivation layer, we have grown a 1000Å PECVD SiO_2 layer for the rf sputtered ZnO films and a 2000Å CVD Si_3N_4 layer for the dc triode sputtered ones. The as-grown ZnO films are transparent with a very smooth surface finish. The grain size of the ZnO films is 0.2--0.5 μm at the rf sputtered films, and no grain boundaries are visible under SEM examination at the dc triode sputtered films.

Fig. 1.9 shows SAW velocity dispersion, which were obtained from the center frequency measurements on the IDTs, along with the theoretical curves. The SAW velocity measured with the knife-edge laser probe is shown in Fig. 1.10.

The value of K^2 is shown in Fig. 1.11 as a function of film thickness normalized with λ. It is seen that the value of K^2 of the dc triode sputtered film is about 1.7 times larger than that of the rf sputtered films as expected from the grain size of the film. The value is approximately 5.7--10.8 times larger than the typical value of bare GaAs (0.07%).

The propagation loss shown in Fig. 1.12 were observed at the frequency range of 230-290MHz, by comparing several transverse scans on the metalized surface with the distance of about 200λ. The measured data shows that the 1.6μm dc triode sputtered film with the passivation layer had the lowest loss and the 4μm rf sputtered film without the

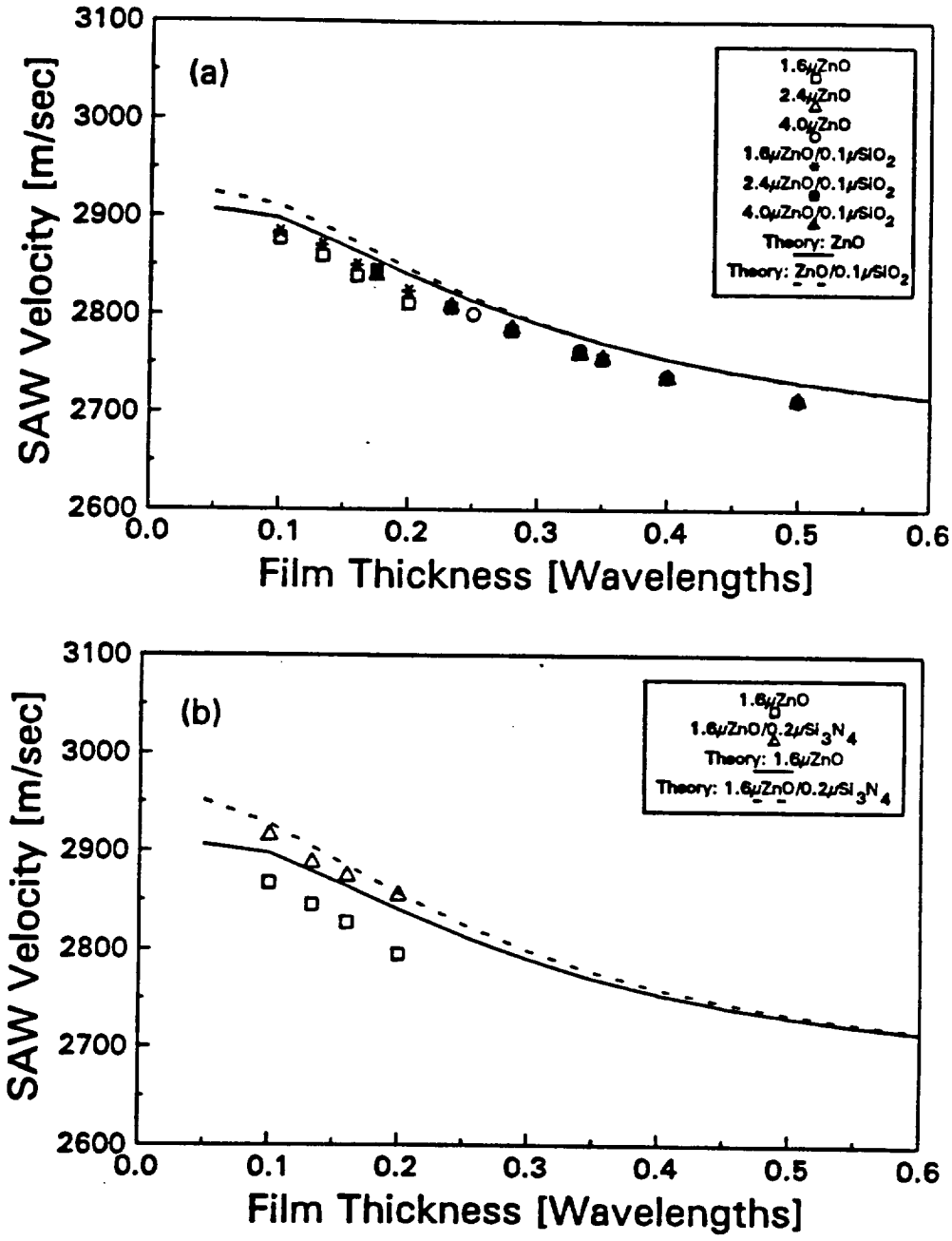


Figure 1.9 SAW velocity obtained from center frequencies of IDTs: (a) rf sputtered film, (b) dc triode sputtered film.

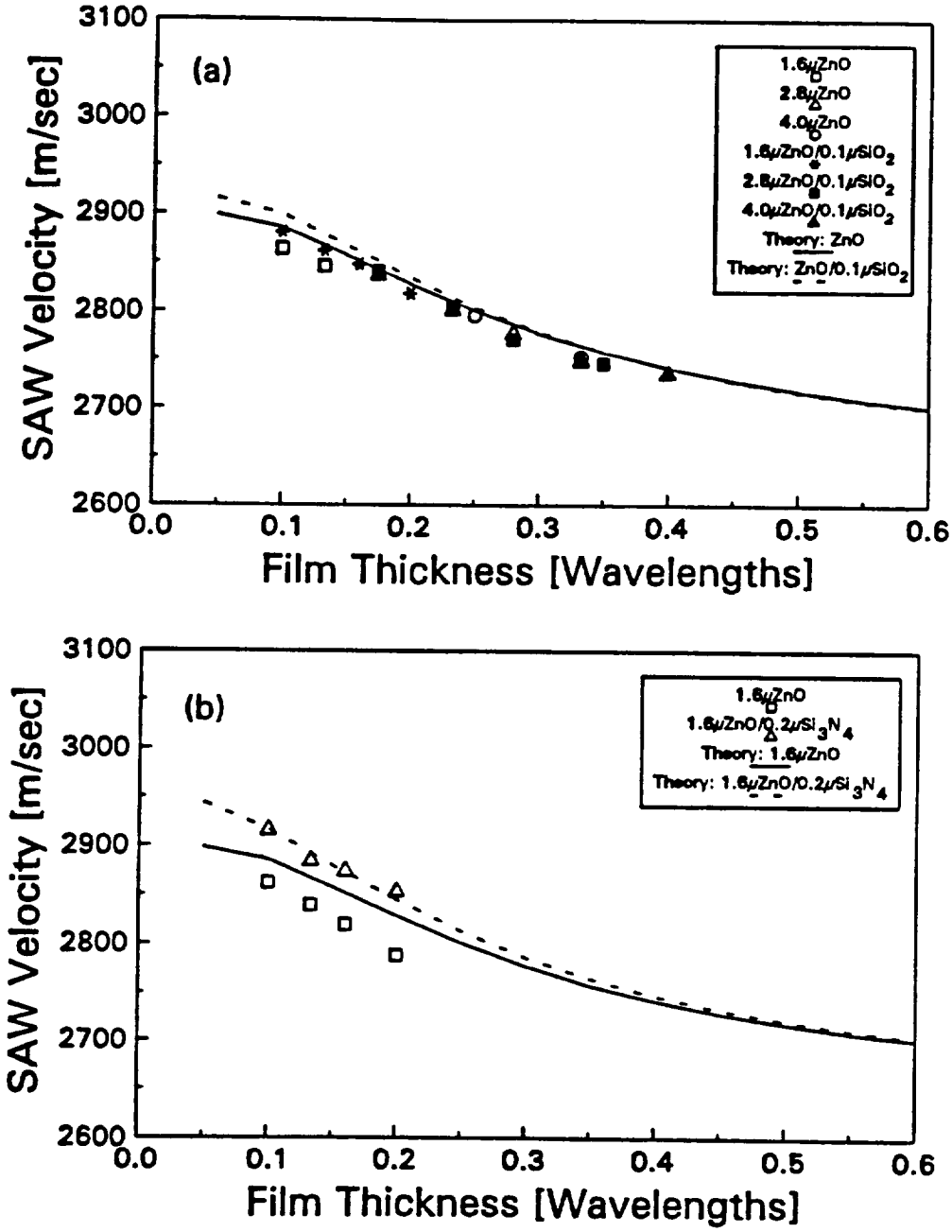


Figure 1.10 **SAW velocity measured by a knife-edge laser probe on metalized surface: (a) rf sputtered film, (b) dc triode sputtered film.**

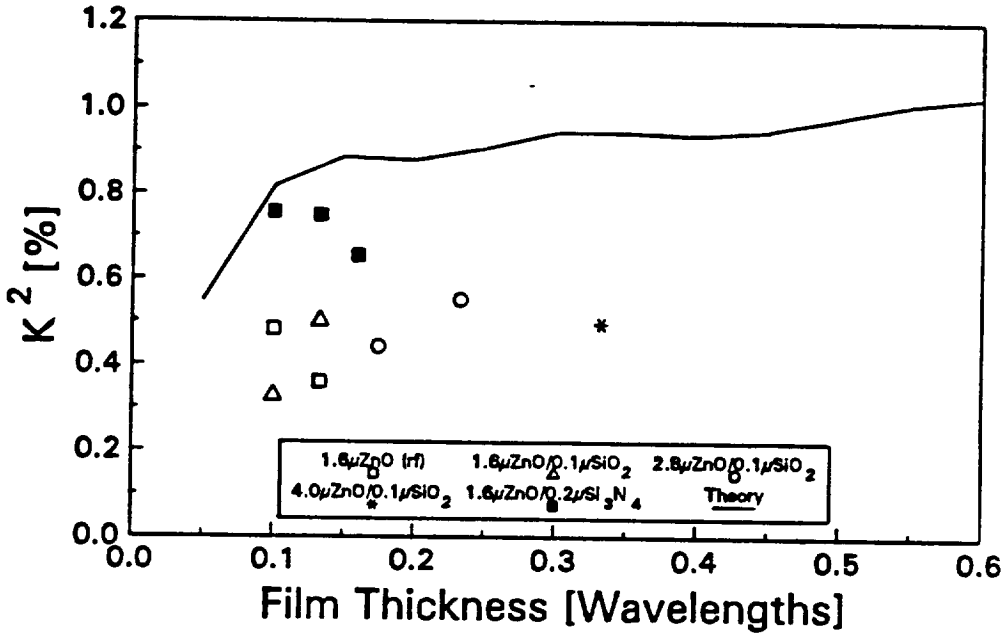


Figure 1.11 Piezoelectric coupling constant.

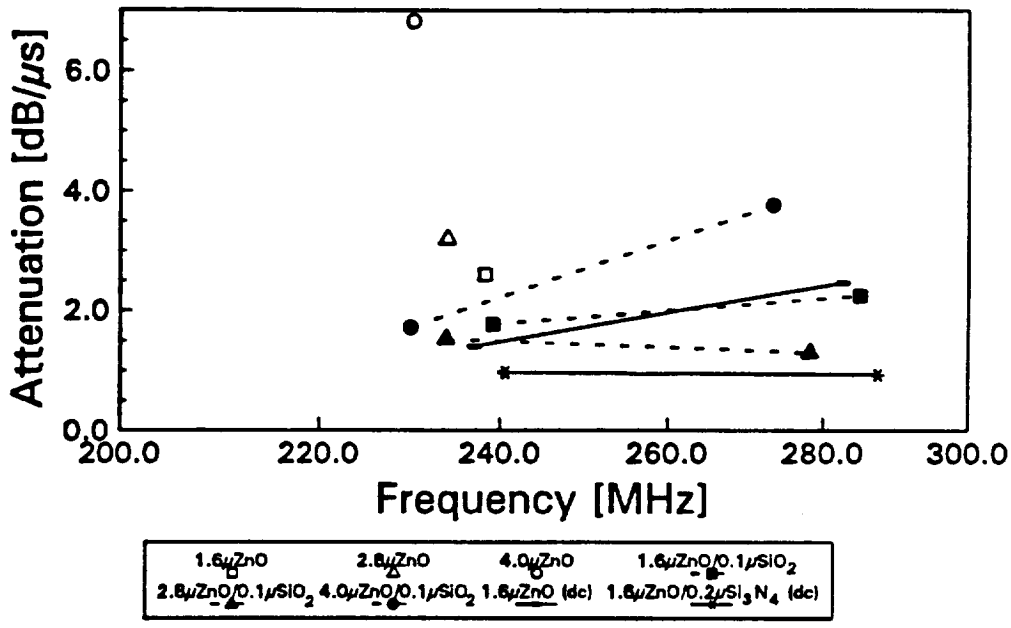


Figure 1.12 Propagation loss at the frequency range of 230-290MHz.

passivation layer the highest loss, which is comparable to the measurement on the other substrates [8, 9]. The passivation layer had a noticeable effect on both sputtered films especially for the rf sputtered ones. It should be noted that the loss of the film is not severely worse than that of bare GaAs substrate, which has the values of 0.323 and 0.567 dB/μs, for 200 and 300MHz, respectively [10], in spite of the diffraction loss.

The reflectance of the multilayered media to the laser probe can be obtained using the ellipsometry theory [11] and are listed in Table 1.1 with the experimental readings of the dc potential of the photodiode, which detects the laser probe, at the laser power of 0.3W. Note that the magnitudes of the dc potential are directly proportional to the theoretical values of R. This would indicate that the scan data on the free ZnO filmed surface over -1.0V shows the profile of the particle displacement on ZnO/GaAs interface rather than ZnO film surface since ZnO crystal has reflectance of only 0.11.

The substrates investigated for the velocity surface were 1.6,2.8, and 4.0μm rf sputtered ZnO films with 0.1μm thick SiO_2 passivation layer and 1.6μm dc triode sputtered ones with and without 0.2μm thick Si_3N_4 passivation when the acoustic wavelength, λ, was 12μm. The typical transverse scan data measured on 250Å thick aluminum-metalized and free surfaces of 1.6 and 2.8μm rf-sputtered ZnO/GaAs and 1.6μm dc-triode-sputtered ZnO/GaAs, and bare GaAs are shown in Fig. 1.13 (a)-(g) where the aperture of the IDT was 8.3λ. The two transverse scans were separated by a distance of 200λ. Note that the diffraction of the ZnO film shown in Fig. 1.13 (a)-(f) is much larger than that of bare GaAs, which clearly shows an autocollimating beam profile in Fig. 1.13 (g). Considering c-oriented single ZnO crystal is isotropic on its basal plane with a value of V=2681m/s, one can expect

Table 1.1 **Theoretical reflectance of multilayered media to the laser probe (wavelength = 5145Å) and experimental reading of dc potential of the photodiode, which detects the intensity of the laser probe at 0.3W power.**

Media surface	Reflectance	Laser probe intensity [V]
Aluminum metalized	0.92	-2.3 ~ -2.6
1.6μm ZnO/0.2μm Si_3N_4/GaAs	0.0~0.37	~ -0.3
1.6~4.0μm ZnO/0.1μm SiO_2/GaAs	0.08 ~ 0.58	-0.1 ~ -1.5
Single GaAs	0.38	~ -1.0
Single ZnO	0.11	N/A

Table 1.2 **Ansiotropic factor of 0.13 and 0.23λ thickness of ZnO film. The values are obtained by curve fitting with a least-square method. The values in the parenthesis are for the short surface.**

ZnO thickness	Sputtering method	Passivation	Theory	Experiment
0.0 (bare GaAs)	-	-	0.22	0.45[a]
0.13λ	rf	0.1μm SiO_2	-0.13 (-0.16)	-0.18 (-0.17)
0.13λ	dc triode	0.2μm Si_3N_4	-0.13 (-0.16)	N/A (-0.19)
0.13λ	dc triode	None	-0.14 (-0.17)	-0.22 (-0.4)
0.23λ	rf	0.1μm SiO_2	-0.44 (-0.56)	-0.71 (-0.55)

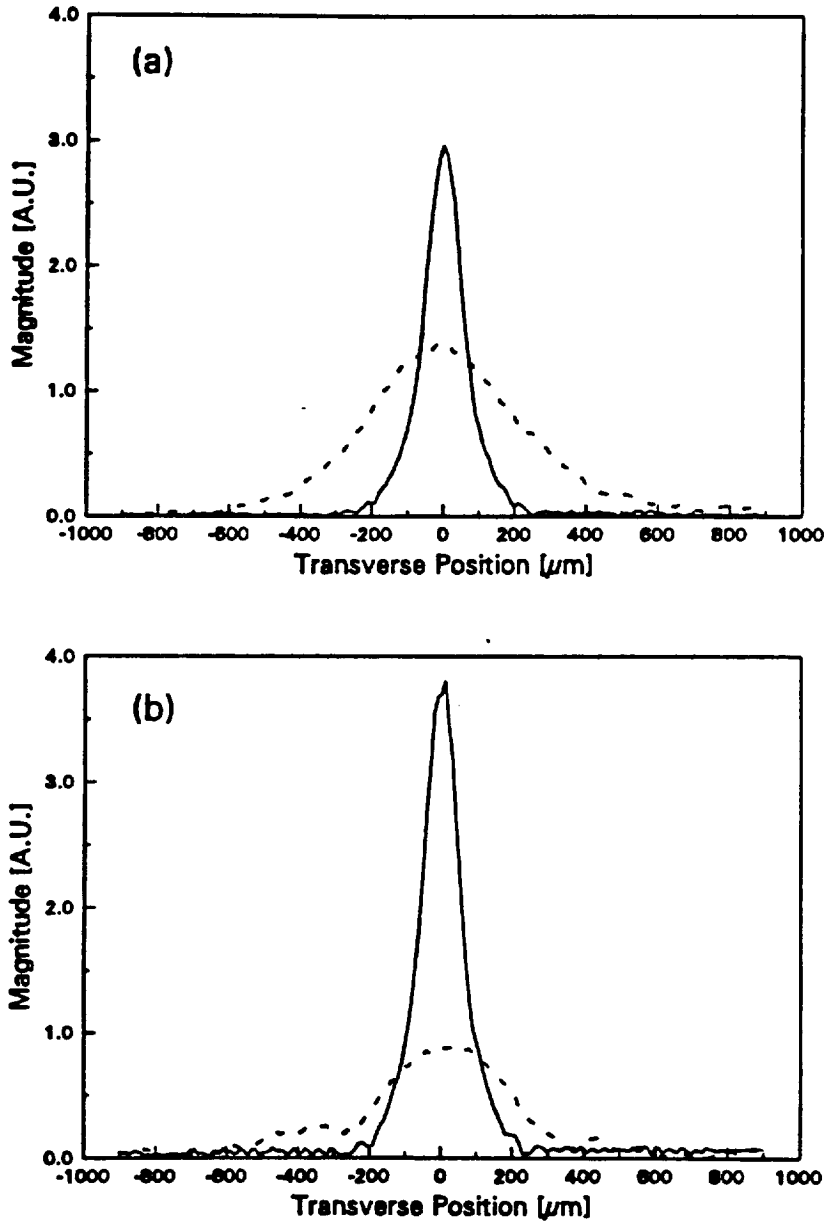


Figure 1.13 **Beam profiles are separated by a distance of 200λ. The solid line represents the scan near the IDT and the dotted line represents that of 200λ apart. (a) metalized and (b) free surface of 1.6μm rf sputtered ZnO, (c) metalized and (d) free surface of 2.8μm rf sputtered ZnO, (e) metalized and (f) free surface of 1.6μm dc triode sputtered ZnO, (g) bare GaAs.**

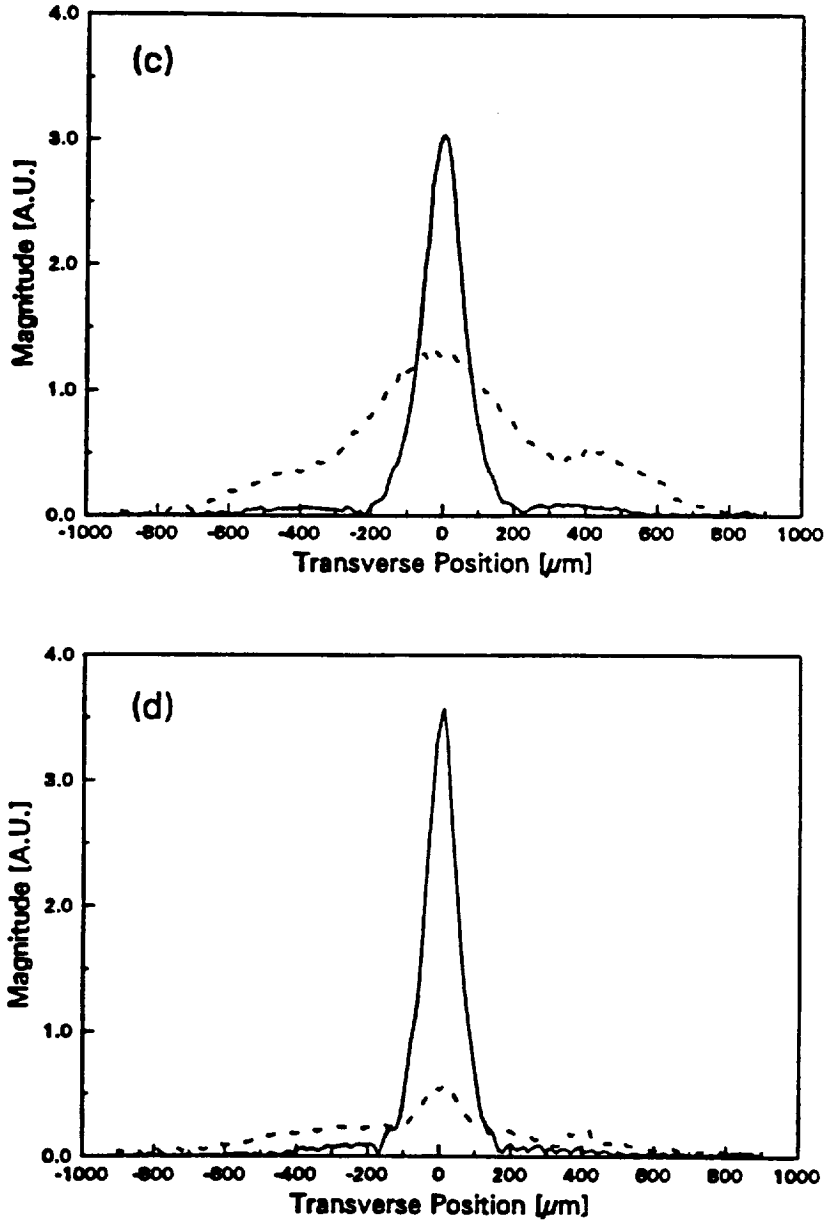


Figure 1.13 **(Continued) Beam profiles are separated by a distance of 200λ. The solid line represents the scan near the IDT and the dotted line represents that of 200λ apart. (a) metalized and (b) free surface of 1.6μm rf sputtered ZnO, (c) metalized and (d) free surface of 2.8μm rf sputtered ZnO, (e) metalized and (f) free surface of 1.6μm dc triode sputtered ZnO, (g) bare GaAs.**

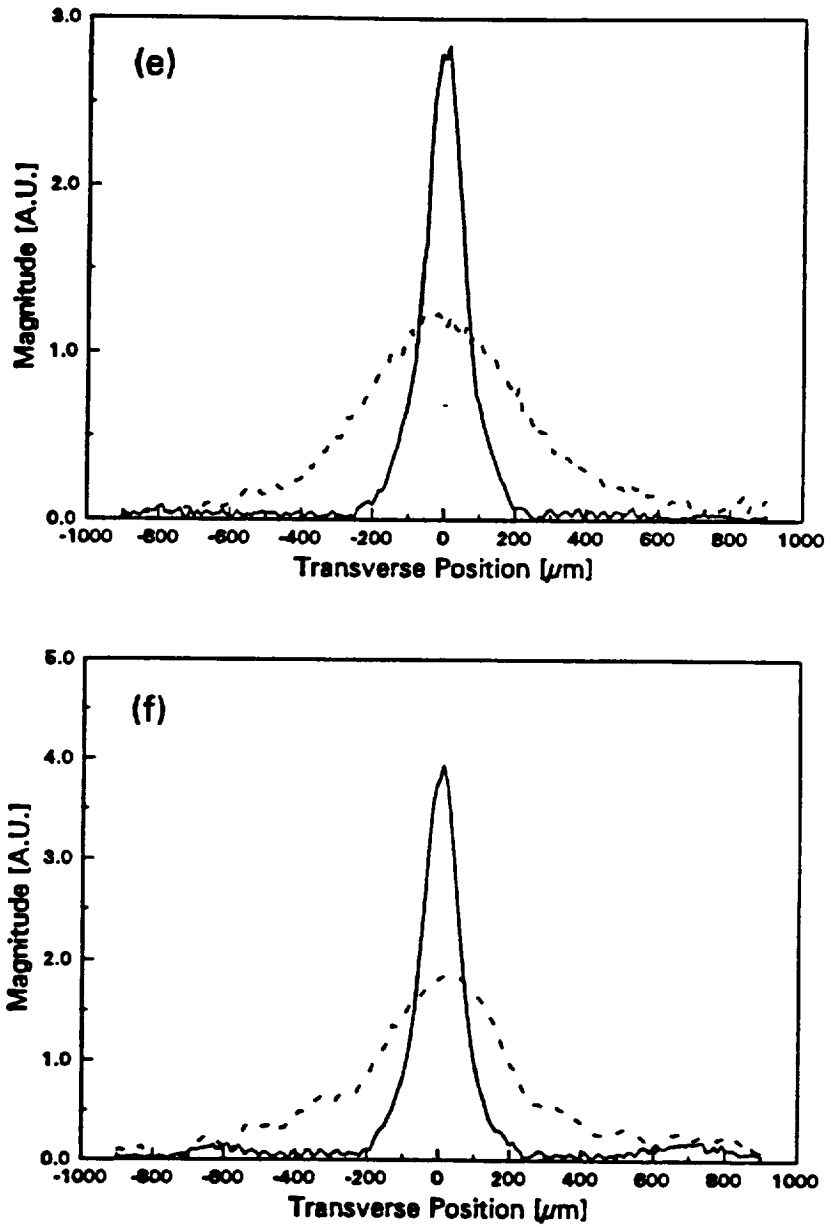


Figure 1.13 **(Continued) Beam profiles are separated by a distance of 200λ. The solid line represents the scan near the IDT and the dotted line represents that of 200λ apart. (a) metalized and (b) free surface of 1.6μm rf sputtered ZnO, (c) metalized and (d) free surface of 2.8μm rf sputtered ZnO, (e) metalized and (f) free surface of 1.6μm dc triode sputtered ZnO, (g) bare GaAs.**

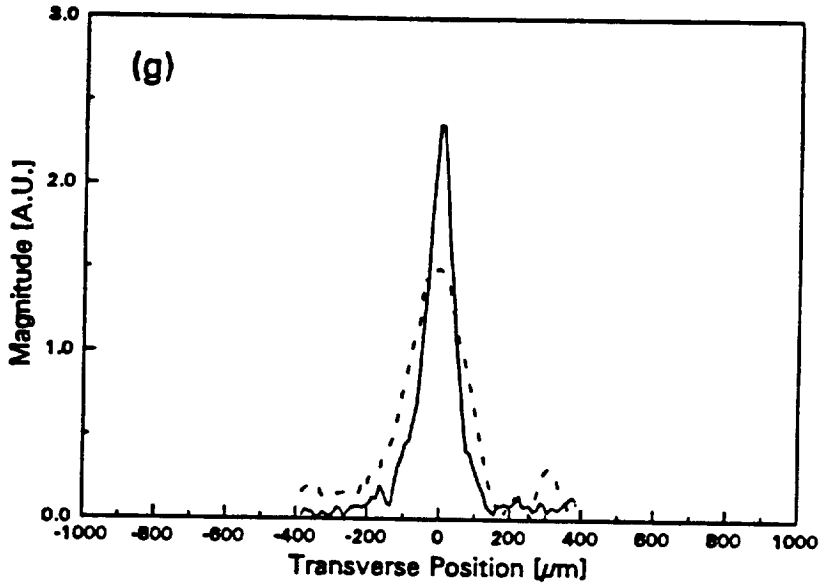


Figure 1.13 (Continued) Beam profiles are separated by a distance of 200λ. The solid line represents the scan near the IDT and the dotted line represents that of 200λ apart. (a) metalized and (b) free surface of 1.6μm rf sputtered ZnO, (c) metalized and (d) free surface of 2.8μm rf sputtered ZnO, (e) metalized and (f) free surface of 1.6μm dc triode sputtered ZnO, (g) bare GaAs.

that the beam of ZnO/GaAs is spread more than that of GaAs. The attenuation of the free surface is much larger than that of the metalized surface particularly for the 2.8μm rf-sputtered ZnO film while this is not noticeable for the dc-triode one. This indicates that the dc triode sputtered film would be more evenly contacted with the substrate than the rf sputtered one. It can be inferred that a lack of even contact at the film and substrate interface would cause a loss of SAW energy in the GaAs substrate.

The theoretical velocity curves of the ZnO film with a 0.1μm SiO_2 passivation layer are shown in Fig. 1.14 (a) as a function of the ZnO film thickness normalized to λ. They were calculated using the Laguerre polynomial technique when the order of expansion was 15. Note that the SAW velocity curves are bending upward, and this is in contrast with that of the bending-downward curvature of the bare GaAs shown together. The effect of the passivation layer is shown in Fig. 1.14 (b) for the ZnO thckness of 0.13λ.

Applying the ASPW theory to the transverse scans produced velocity surfaces shown in Fig. 1.15. The ASPW theory assumes that the plane wave propagates in the media, and the calculation of the theoretical curves are based upon the material constants of the single medium instead of unknown constants of the film. Nevertheless, is should be noted that there is close agreement between Fig. 1.14 and 1.15.

As shown in Fig. 1.15, the parabolic approximation for the 0.33λ thick ZnO film is not appropriate since the curvature is almost flat (*i. e.* isotropic) near the zero angle. Therefore, the values of b for the 0.13 and 0.23λ thickness were obtained from a least-square's curve fitting and are listed in Table 1.2 for the comparison between the theory and the experiment (in fact, the result of the ASPW theory).

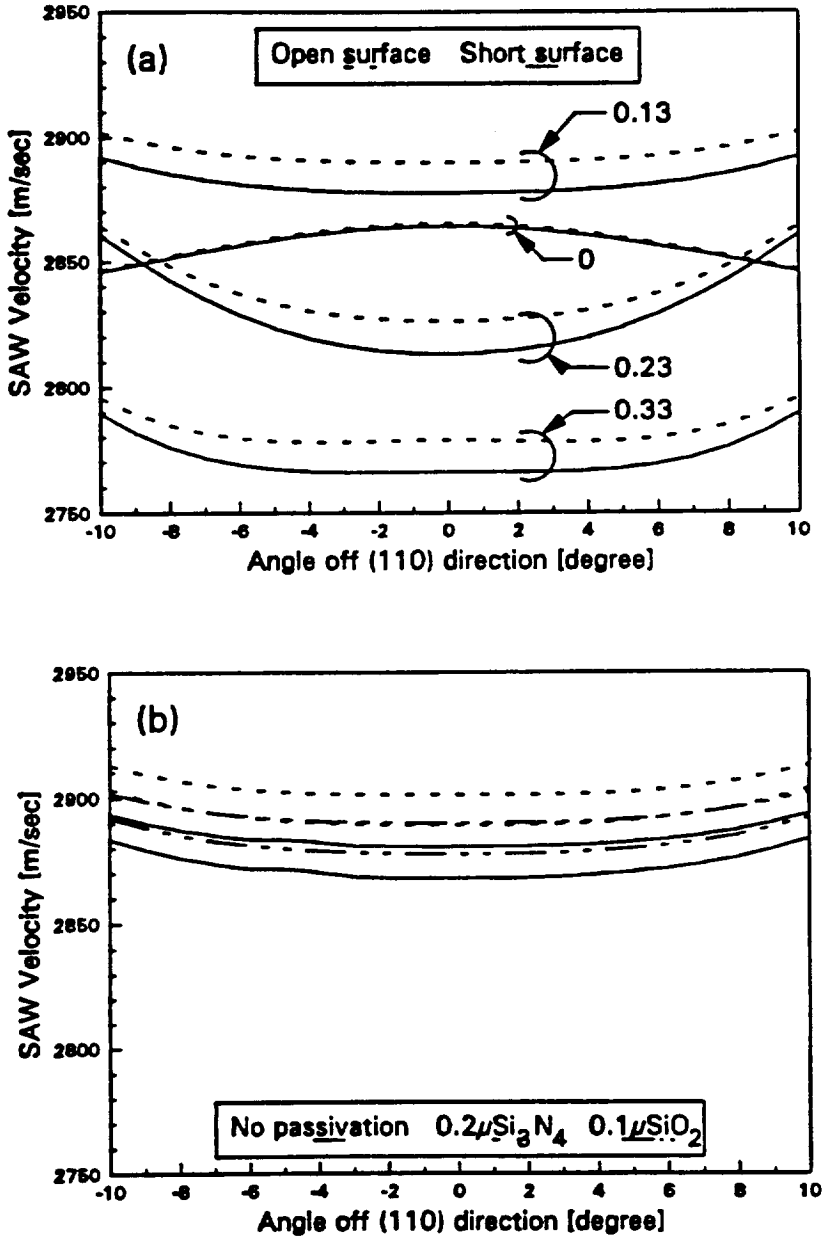


Figure 1.14 **Theoretical velocity surfaces obtained using Lagurre polynomial technique. Numbers indicate the thickness of the ZnO film normialize by λ. (a) effect of ZnO film thickness, (b) effect of passivation for 0.13λ thick ZnO film.**

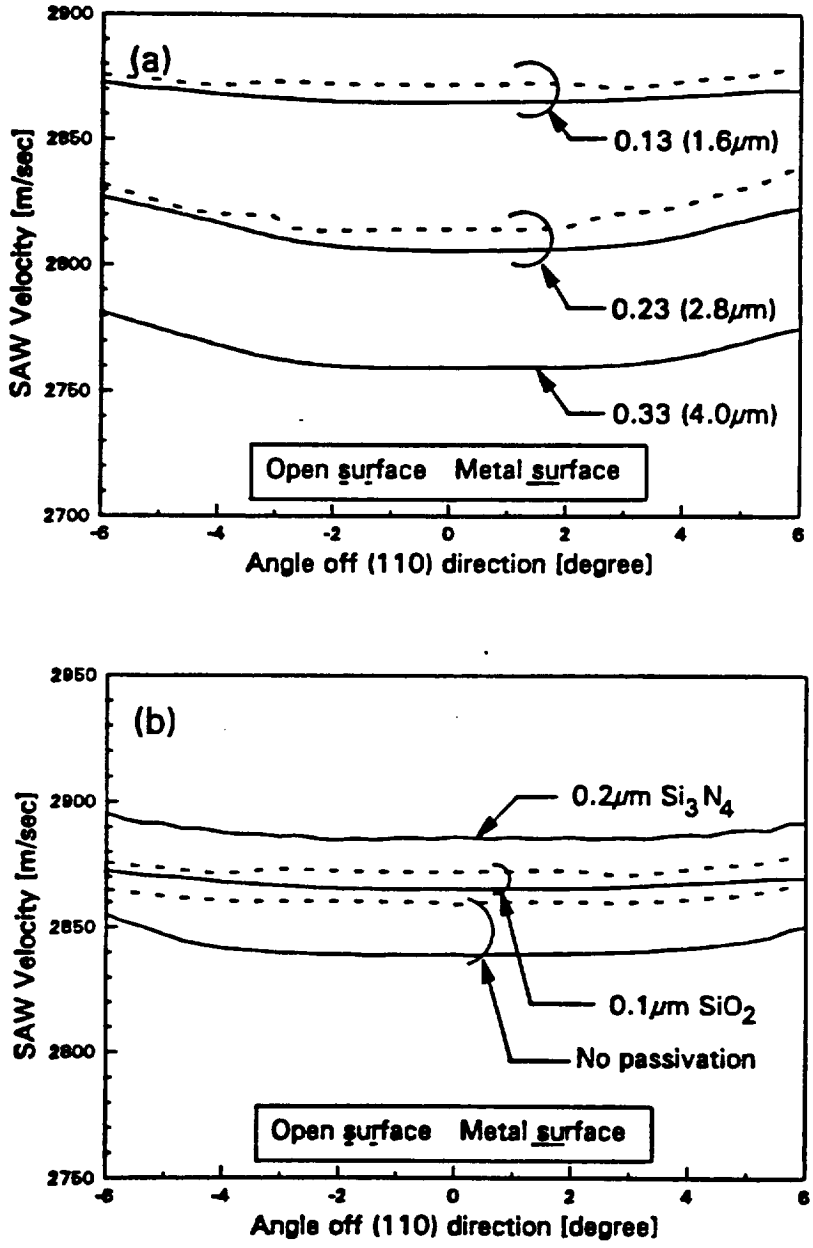


Figure 1.15 Experimental velocity surfaces obtained applying angular spectrum of plane wave theory to transverse scans. Numbers indicate the thickness of the ZnO film normialize by λ. (a) effect of ZnO film thickness, (b) effect of passivation for 0.13λ thick ZnO film.

In summary, the SAW properties on both rf and dc triode sputtered ZnO films on {100}-cut <110>-propagating GaAs have been measured and compared to theoretical calculations. The measured SAW velocity corresponds well with the theoretical calculation using a Laguerre polynomial technique. The passivation layer improves the ZnO film quality appreciably for both sputtering methods. The best quality of film observed has been 1.6μm dc triode sputtered ZnO film with 2000ÅSI_3N_4, for which the propagation loss was 0.9-1.0dB/μs at 240-280MHz. Its value of K^2 would be lager than that of the film without the passivation layer, 0.65-0.75%. Compared with bare GaAs, this particular film substrate has approximately 0.6% lower SAW velocity, at least 10 times lager K^2, and 0.6dB/μs more propagation loss.

Velocity surfaces have been obtained using an angular spectrum of plane wave theory and compared with theoretical ones. The results of bending upward curverture have been shown in good agreement with the theory, implying that the ZnO/GaAs has more rapid diffraction than bare GaAs.

Employing a wide aperture of the IDT or a waveguide will be a solution to overcome the high diffraction situation on ZnO/GaAs.

2.0 Work Accomplished During This Period: Theoretical Program

During the first six month effort of the first contract year of funding, the theoretical work has focused on the design and optimization of the avalanche photodiode, APD, the development of a far more advanced simulator for studying impact ionization and the workings of the APD, and the development of a model for studying the charge transfer transistor. Each of these projects will be discussed in detail below.

2.1 APD Design and Optimization

Our goal is to develop a relatively high gain, ultra-low noise, low-voltage APD for use in an HDTV camera. The most promising candidate for this task is the doped barrier and doped quantum well APDs [12, 13]. The basic structure of the doped quantum well devices consists of alternating layers of wide and narrow bandgap material with a p-i-n region formed within the wide bandgap layer. Each unit cell contains five separate layers. Though the original design [12, 13] offers the potential of high gain at low noise and operates at low voltage, optimal realization of the device may be difficult to achieve. Experimental measurements to date have shown ultra-low noise performance but only at low gain levels, i.e. less than 5. At higher gain in the structures studied to date, the experimental results show that the noise increases dramatically ultimately approaching the noise of an APD made from bulk GaAs material. It is believed that the increased noise at high gain levels arises from the failure to fully deplete all of the stages of the device due to an imbalance in the n and p-type doping concentrations present within each stage. As a result, only some of the stages within the device become fully depleted by the action of the reverse bias. Further increase in the reverse bias leads to an increase in the overall field of the device. Consequently, the breakdown at higher bias arises predominately from the action of the overall electric field and not from the built-in p-i-n layers. This leads in turn to an increase in the hole ionization rate resulting ultimately in comparable electron and hole ionization rates in the device.

The primary cause of the inability to fully deplete all of the stages of the device is believed to be due to the difficulty of balancing the very high doping concentrations of the p

and n layers within the built-in junctions. Since the required doping concentrations are very high, even small variations in their values can lead to significant charge imbalance. It is important then, to develop a design in which control of the doping concentration can be enhanced enabling the full depletion of the active region. If all of the stages of the device can be fully depleted, then electron ionization should occur within each stage greatly increasing the gain of the overall device.

In this section and in the enclosed publications, we discuss a new variation of the original doped quantum well and barrier APD structures which utilizes delta-doping in the built-in junctions. Single sheets of dopants are selectively added to form p-i-n junctions within either the AlGaAs barrier or GaAs well regions. It is expected that the device can be more easily depleted since charge balance within each stage is more readily achieved. Through a judicious choice of the doping concentrations within each sheet as well as the other parameters, low noise operation at higher gain should be possible.

Two different device structures were examined. A sketch of the devices is shown in Figure 2.1. In the first device considered, the delta doping is placed in the GaAs layers. In the second structure, the delta doping is confined completely within the AlGaAs. Therefore, the two designs are similar except for the fact that in the second structure, the doping layers and intrinsic layer sandwiched between them are formed in AlGaAs rather than GaAs as shown in Figure 2.1.

In the GaAs doped structure, the basic unit cell has five layers made of two different materials. The p and n doped layers are formed within the GaAs layer and are only about one monolayer in width. Under reverse bias, the electrons are accelerated from left to right

in the diagram while the holes move in the other direction.

There are five independent parameters that can be varied that effect the device performance. These are: the overall applied electric field, the built-in electric field which is related to the charge density, the high field layer width, the low field GaAs layer width, and the low field AlGaAs layer width. The high field layer is defined as the layer sandwiched between the two delta doped regions as shown in Figure 2.1. The low field AlGaAs layer is defined as the layer immediately to the right of the p+ contact as shown in Figure 2.1. The low field GaAs layer is the layer placed immediately to the right of the n-type delta doped region. There are two major issues which govern the device performance. First, the electron temperature must be high within the GaAs layer to obtain a high impact ionization rate. Second, the hole temperature within the GaAs layer must be low enough to inhibit hole ionization.

We have examined how each of the above mentioned parameters influences the device performance based on an ensemble Monte Carlo simulation of the electrons and holes within the device structure. The details of our calculations are discussed in the enclosed preprints. However, the results can be summarized as follows. The fundamental tradeoff implicit in the device design is that the doping concentration and high field layer widths must be sufficiently low such that the hole ionization is completely suppressed, yet large enough to cause sizable electron ionization. Under comparable conditions, the GaAs-doped (doped well device) device exhibits gain typically significantly lower than in the AlGaAs-doped device. Our calculations show that the hole ionization rate can be completely suppressed in either device structure, but that the corresponding electron ionization rate is greater in the AlGaAs doped

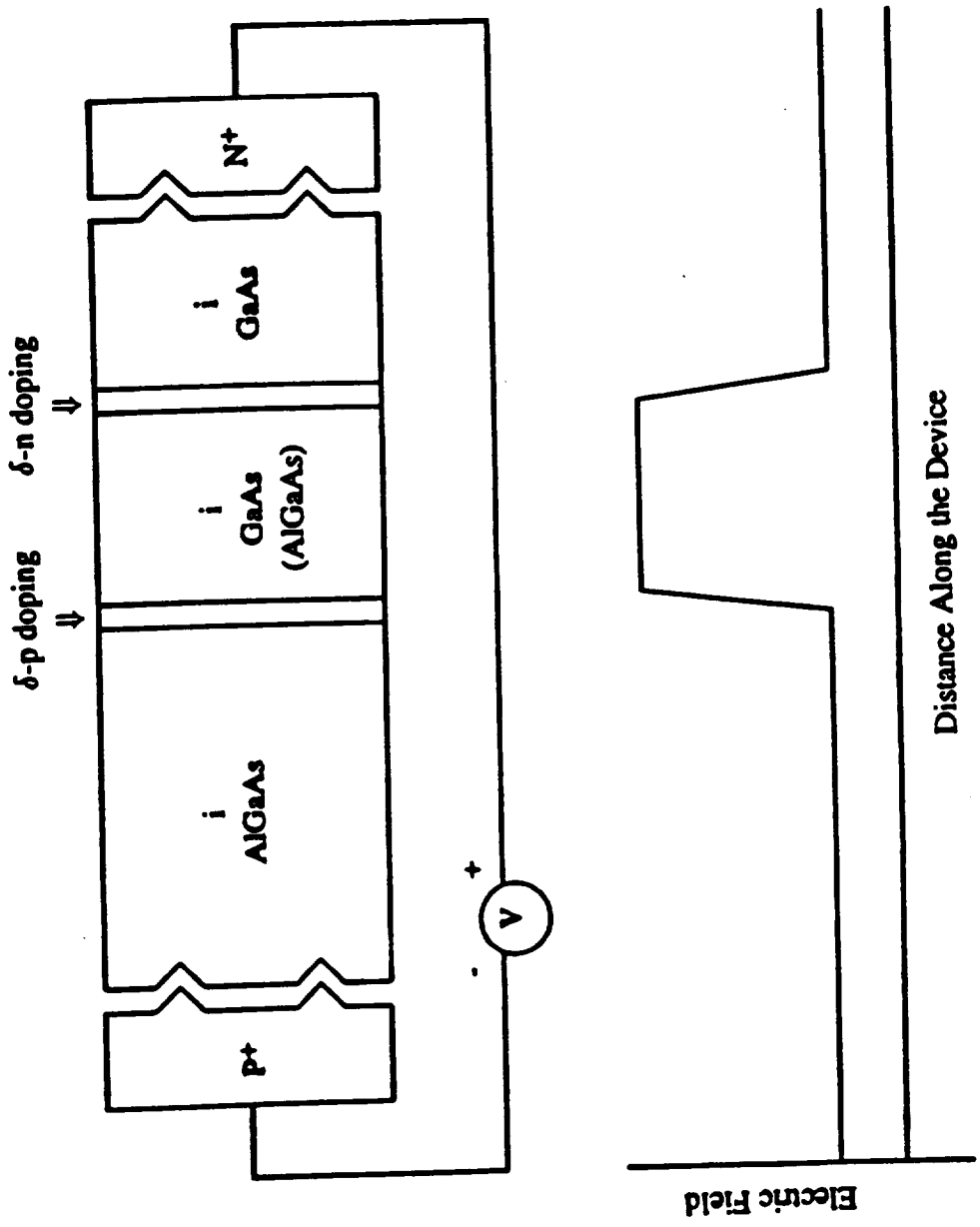


Figure 2.1 Sketch of the basic unit cell of the device along with the electric field profile.

device. Due to the fact that the electron ionization probability per stage is predicted to be only ~ 0.1 (meaning that only one in ten electrons ionizes on average at each stage of the device), in order to achieve the targeted gain of ~ 8, over 20 stages will be required. Depleting this number of stages may prove troublesome.

Though the complete suppression of the secondary hole ionization rate is desirable since it ultimately leads to very low noise performance even at very high gain, it is not always necessary at low gains. The noise in a low gain device does not change greatly with small changes in the hole or electron ionization rates. This can be seen from inspection of Table 2.1. In Table 2.1, the gain, M, and excess noise factor, F_e, are calculated at fixed P and Q for different number of stages, m. As can be seen from the table, the excess noise factor changes very little, almost immeasurably, as the number of stages changes from 9 to 10 or 8 but the gain changes greatly. Therefore, some amount of hole ionization can be tolerated at low device gain without sacrificing noise performance especially if it will lead to a significant increase in the overall device gain.

We examined different structures in which a small amount of hole ionization is present. Table 2.2 illustrates the "best " device configuration and how variations in the applied field, built-in field and high field intrinsic layer width effect its performance assuming that the doping is completely confined within the AlGaAs barrier layers. As can be seen from inspection of Table 2.2, a substantially higher value of the electron ionization probability per stage, P, is obtained. For the specific case considered (that corresponding to the first set of parameters in the table) P is equal to 0.263 while the value of the hole ionization probability, Q, is 0.00046. The corresponding gain and noise in a 9 stage device is

Table 2.1 **Doped barrier device: gain and noise performance as a function of the number of stages present.**

Electron ionization probability P	Hole ionization probability Q	Number of stages m	Gain M	Excess noise factor F_e
0.263	0.00046	9	8.27	1.53
0.263	0.00046	10	10.5	1.545
0.263	0.00046	8	6.52	1.50

Table 2.2 Doped barrier device: effects of variations in device parameters.

Applied Field (kV/cm)	Built-in Field (kV/cm)	Intrinsic Layer Å	P	α	Q x 10^4	β	Trapping
175	450	200	0.263	3.28	0.00046	57.2	7.3
Case 1: Effect of Variation of the applied field:							
165	450	200	0.241	2.98	0.00060	75.2	10.1
185	450	200	0.28	3.52	0.0013	163.4	6.1
Case 2: Effect of Variation of the high field intrinsic layer width:							
175	450	225	0.294	3.55	0.0011	130.1	7.9
175	450	175	0.217	2.8	0.0	0.0	8.8
Case 3: Effect of Variation of the built-in field:							
175	475	200	0.297	3.69	0.00035	43.3	7.2
175	425	200	0.229	2.85	0.00057	71.5	7.2

shown in Table 2.3. It is instructive to compare the gain and noise performance to a device structure in which the hole ionization is fully suppressed. The gain and noise for such a device for a comparable number of stages is also shown in Table 2.3. Clearly, comparison of the two designs shows that a significant improvement in device gain can be attained without much sacrifice in the noise of the device if some residual hole ionization is allowed to occur.

In order to assess the overall performance of the device it is useful to consider how the gain and noise vary with small fluctuations in the device parameters and applied electric field. In our previous studies [14], we have found that variations in the applied electric field, high field layer width and the built-in field (equivalently the doping concentration), have the most dominant effect on the device gain and noise. In Table 2.3, we show how the variations in the applied field, high field layer width, and built-in field of the devices listed in Table 2.2 effect the gain and noise of the base device, defined as the structure operating closest to the optimal operating point (the first device listed in both tables 2.2 and 2.3). It is interesting to note that the noise changes very little as a general rule, however the gain of the devices changes significantly with the different variations. From inspection of Tables 2.2 and 2.3, it is clear that much higher gain at negligible increase in the excess noise of the device can be attained by operating the device with some residual amount of hole ionization. The only drawback to this approach is that the gain can fluctuate significantly with variations in the device parameters and operating bias. This may not present a problem in the overall performance of the detector for the HDTV camera since an overflow transistor follows the detector stage which will remove excess charge anyway. However, this question must still be

Table 2.3 **Doped barrier device: gain and noise performance as a function of changes in the device parameters.**

Electron ionization probability P	Hole ionization probability Q	Number of stages m	Gain M	Excess noise factor F_e
Base Device:				
0.263	0.0046	9	8.27	1.53
Zero Hole Ionization Device:				
0.110	0.0	9	2.56	1.49
Case 1: Effect of Variation of the Applied Field:				
0.241	0.0006	9	7.07	1.55
0.28	0.0013	9	9.58	1.54
Case 2: Effect of Variation of the High Field Layer Width:				
0.294	0.0011	9	10.5	1.50
0.217	0.0	9	5.85	1.53
Case 3: Effect of Variation of the Built-in Field:				
0.297	0.00035	9	10.5	1.50
0.229	0.00057	9	6.47	1.54

resolved and will be examined in the next six months.

2.2 Development of an Advanced Theory of Impact Ionization and its Application to the Study of APDs

In the second part of the project, we have made extensive progress towards improving the accuracy of our simulators for studying the workings of the APDs. Specifically, we have developed a new approach to formulate the impact ionization transition rate which includes the k-dependence of the ionization rate. Presently, we are calculating the transition rate for bulk silicon in order to compare with experimental measurements and previous theories [15, 16]. Due to the extensiveness of these calculations, the results are not yet known. However, we expect to have the solution for bulk silicon and subsequently for bulk GaAs within the next few months. The inclusion of the k-dependence of the ionization transition rate is expected to have a substantial effect on the calculations. With the additions currently being worked on, our simulators can be made sufficiently complete that they will enable a far more reliable assessment of the workings of multiquantum well devices.

Once we have calibrated our new model using the k-dependent formulation of the ionization rate, it will be used to restudy the ionization rate in a simple GaAs/AlGaAs multi-quantum well APD as well as the doped barrier and doped quantum well devices. The new model should give a far more accurate prediction of the electron and hole ionization rates in these devices enabling an assessment of the optimal performance of the doped quantum well devices. This in turn will aid us in "fine-tuning" the doped quantum well structure for use in the HDTV camera.

We have also completely revised our hole simulation code. The most important revision is that the hole-phonon scattering rate is now calculated numerically taking into

account the warping of the valence bands, i.e. heavy hole, light hole and split-off bands. The hole-phonon scattering rate is calculated along three principal axes in the material at 50 meV intervals. Both the nonpolar optical and the polar optical scattering events are included. Acoustic phonon scattering is neglected since it is typically much weaker than either the nonpolar optical or polar optical scattering especially at high energies at which impact ionization occurs. The scattering rates are calculated by integrating numerically over the possible final states determined from a k o p calculation of the band structure. Below 0.6 eV of energy the scattering rates are determined to only first order in perturbation theory. Above 0.6 eV, the scattering rates are calculated using a full order quantum mechanical approach [16]. Our calculations have shown that the hole-phonon scattering rate is not greatly anisotropic. Nevertheless, it is useful for completeness to reformulate the hole-phonon scattering rate numerically to ensure accuracy in the calculation.

Finally, we have also greatly improved the interpolation scheme for finding the energy in both the electron and hole simulators. The error in determining the energy from the k-vector is no greater than 2-3 meV, a great improvement over that in our previous simulators. Therefore, with the improvements in the energy interpolation, phonon scattering rates, and the impact ionization transition rate the latest versions of the simulators should produce far more accurate results enabling a far better assessment of the optimal performance of the APD device. During the next six months of the project, we will use the new version of the simulators to calculate the impact ionization rates in bulk and superlattice devices.

2.3 Theoretical Study of the Charge Transfer, Collection and Overflow Transistor

The third phase of the theoretical work unit for the first six months is the

development of a modeling tool for the study, and optimization of the charge transfer, collection and overflow transistor. We have succeeded in developing a two-three dimensional drift-diffusion solver coupled with the Poisson equation. Certain specific features have been added to our model which are not commonly available in commercial drift-diffusion solvers. Specifically, our solver contains a tunneling formulation as well as thermionic emission. The inclusion of both tunneling and thermionic emission into the model enables the complete study of Schottky barriers and heterojunctions. To our knowledge, we are one of the first groups to develop a complete solver including tunneling. This improvement is important to the optimization of the charge transfer, collection and overflow transistor since a tunneling barrier is being considered within that device to control the charge transfer under bias.

In addition, we are working closely with the experimental effort to design experiments which will aid in the evaluation of the charge transfer, collection and overflow transistor. In this way, our model is tailored from the beginning to produce results which can be directly compared to experiment. During the next six months we will apply our model to the study of the operation of the transistor and make comparisons to experiment in an attempt to develop an optimal structure.

3.0 Work Accomplished During This Period: Materials and Fabrication Program

During this period work has progressed well in developing advanced fabrication processes for the acoustic charge transport device, and a charge transfer device in AlGaAs heterostructures. Work was also continued in characterizing avalanche photodiode devices and refining MBE growth processes for larger scale, 2" diameter wafers.

3.1 Heterojunction Acoustic Charge Transport Device Fabrication

Excellent progress has been made in the fabrication of heterojunction acoustic charge transport (HACT) devices during this reporting period. Specific tasks which have received emphasis this period include mask set revisions, ohmic contact optimization, pattern delineation, HACT fabrication and device assembly. These tasks are discussed in detail below.

3.1.1 Ohmic Contact Experiments

During the testing of the first materials characterization test devices, it was discovered that the semiconductor contact resistance, which was measured from specific ohmic test structures, was in excess of 10 megohms. Possible reasons for this problem are: first, the ohmic contacts could be bad and another recipe should be used, or second, due to the structure of the material, it may not be possible to measure ohmic contact resistance even though the contacts are good.

To identify the problem, a sample of HACT material doped to $2x10^{18}$ cm^3, one order of magnitude higher than required for HACT devices, was processed with the standard ohmic recipe for ohmic contacts. The standard recipe consists of 800Å AuGe (88/12), 100Å Ni, and 1000Å Au rapid thermal annealed at 365°C for 30 seconds. With the higher doping, good ohmic contacts should be measurable. The average contact resistance was measured to be 0.049 ohm-mm, proving that the process was good. Therefore, it was decided that, because of the undoped cap layer and the few carriers in the channel, contact resistances could not be measured on HACT material doped at 10^{17} cm^3.

Since none of the processed devices were electrically operational, it is possible that

the ohmic contacts did not diffuse far enough into the material and did not contact the quantum well. However, based on the above experiments this is not likely. Additional experiments are needed and are being designed to resolve this problem.

3.1.2 Device Fabrication

During this reporting period, five HACT wafers and one materials characterization wafer were processed and tested. The materials characterization sample included test structures for ohmic contact resistance, Schottky diodes, CV measurements, sheet resistance, Hall samples and electron mobility. Two of these devices were also included on the HACT mask set.

Five HACT wafers were processed and tested as shown in Table 3.1. Wafer processing steps included mesa patterning and subsequent etching, ohmic contact patterning, ohmic metal deposition, lift-off and alloying. Transducer fingers and sensors were formed by a lift-off process using aluminum metallization. Schottky gates and pad metallization were patterned again using a lift-off process. Figure 3.1 shows a completed HACT chip.

3.1.3 Device Assembly

After wafer processing was completed, the wafers were coated with thick photoresist to protect the surface, and diced into individual devices using a dicing saw. The photoresist was removed with acetone and extreme care was taken to avoid scratching the fragile aluminum transducer metallization. HACT chips were mounted in 30 pin flat-pack packages using conductive epoxy and were wire bonded with a thermosonic wedge wire bonder, as shown in Figure 3.2.

Table 3.1 Status of HACT Wafers Processed.

Wafer #	Doping	AlGaAs Thickness	Comments
MC-1	$Xx10^{17}$	700Å	Material characterization data taken.
B92-75	$5x10^{17}$	700Å	Acoustic measurements only
B92-81	$3.5x10^{17}$	700Å	Acoustic measurements only
B92-72	$2x10^{17}$	700Å	Acoustically sound, but devices did not function electrically.
B92-93	$2x10^{17}$	700Å	Acoustically sound, but devices did not function electrically.
B92-82	$3.5x10^{17}$	700Å	

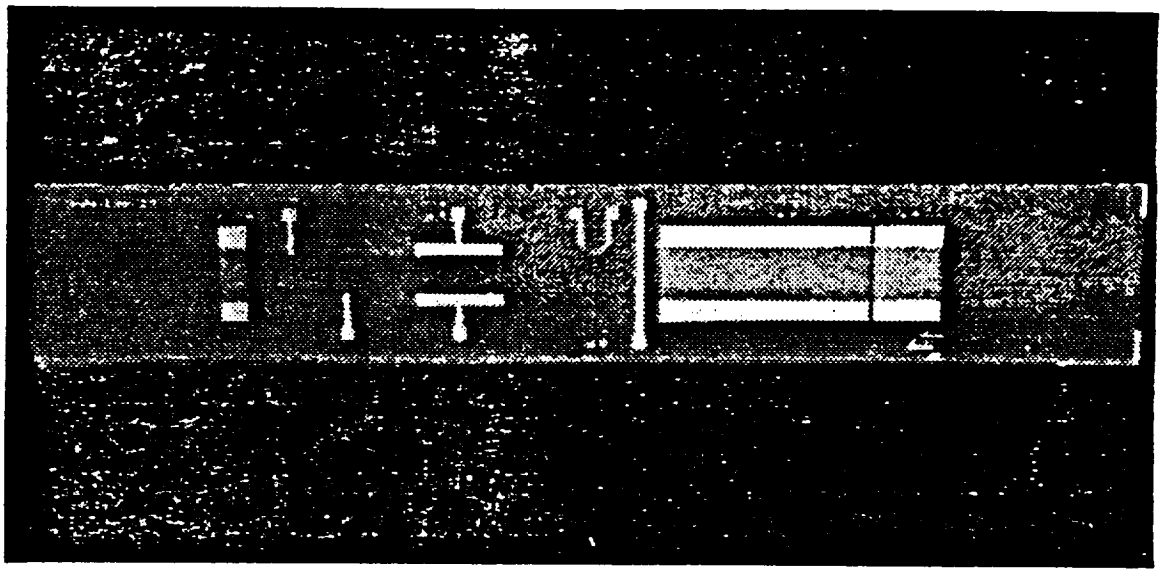


Figure 3.1 A completed HACT device.

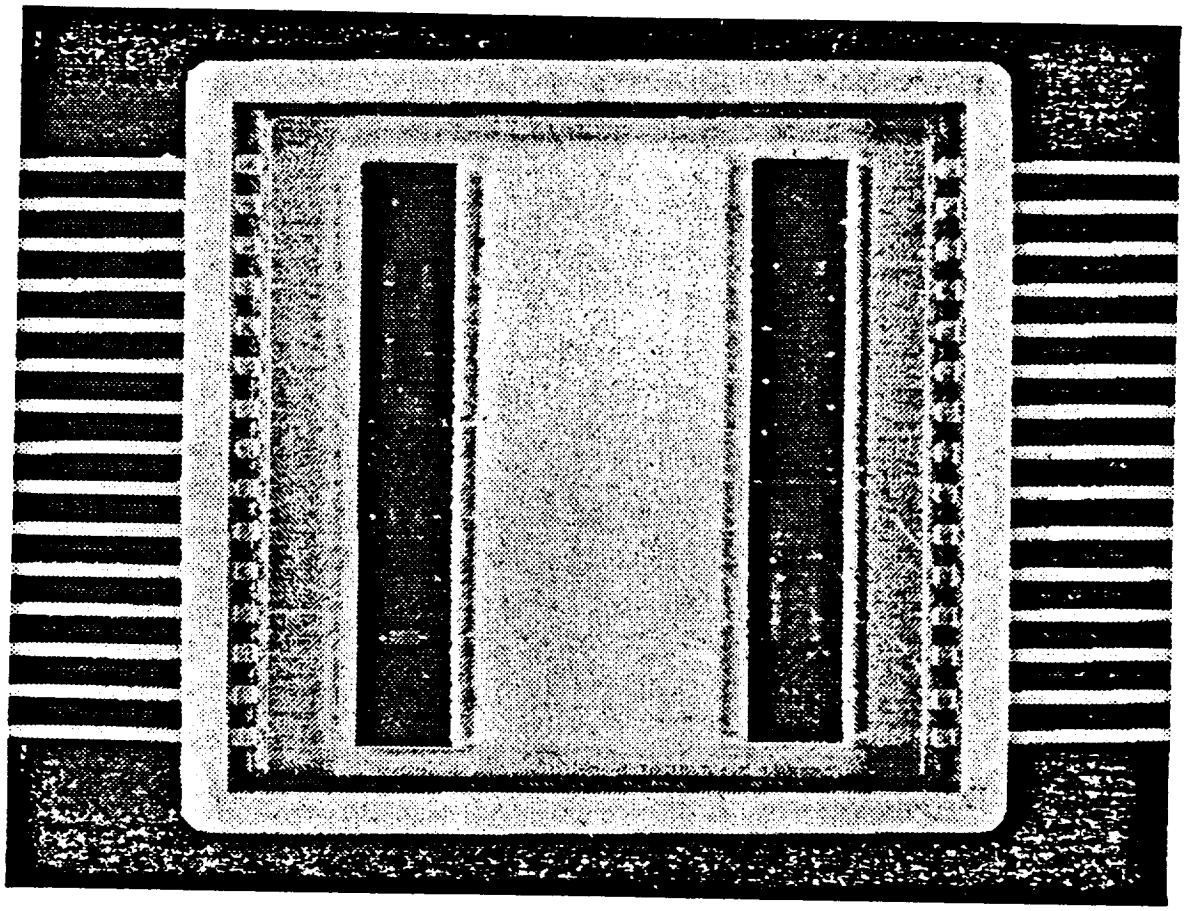


Figure 3.2 Packaged HACT devices.

3.1.4 Electrical Measurements

The first two samples, listed in Table 3.1, were used for acoustic measurements only. These devices resonated at 188 MHz which was very close to the designed frequency. The transducer efficiency, the measure of electrical power that was converted into acoustic power, was also close to the designed value.

The three latest samples were diced and packaged in a 30 pin flat-pack. As shown in Figure 3.2, two devices were bonded into one package and the package was then soldered into a circuit board for testing. The devices on these three samples functioned acoustically, but not electrically. This indicates that charge was not being injected into the quantum well and several theories are currently being investigated to identify the problem.

It is likely that the sheet resistance of the material is too high for HACT devices. The material that has been processed so far has a measured sheet resistance in excess of 110 kohms/cm^2. This is believed to be ten times higher than the required HACT sheet resistance. Currently, the sheet resistance is measured, post-process, with test structures on the wafer. To eliminate bad material, methods of measuring the sheet resistance before the processing are being developed.

The second possibility is that the ohmic contacts are not diffusing down into the quantum well. This means that the charge is not being injected into the well. Other ohmic contact metallizations, alloying times and temperatures are currently being tested to resolve this problem.

3.1.5 Future Plans

In the immediate future, experiments will be preformed to determine why charge was

not being transported in some of the previously fabricated devices. By using a laser to inject charge into the input of the HACT, it can be determined whether the sheet resistance of the material is too high or the ohmic contact recipe needs to be altered.

Further work is also planned to determine exactly what combination of doping levels and ohmic contact processes are needed to electrically inject charge into the HACT so that this testing procedure can be used to refine the HACT structure before it is integrated into the HDTV imager.

3.2 Fabrication and Characterization of Charge Transfer and Overflow Devices

In this six month period, rapid progress was made in the fabrication of working charge transfer and overflow devices (CTD) on in-house grown molecular beam epitaxy GaAs-AlGaAs material structures. The section presents the advances made in the fabrication and characterization of the CTD's. The section begins with a description of improvements made in the device fabrication process which was originally described in detail in the last six month report. After this discussion, enhancements to be made to the CTD mask set are presented. These enhancements are a result of the knowledge gained through the first series of CTD process runs, as described in the last six month report, and the second and third series of CTD process runs described in this report.

3.2.1 Fabrication of CTD Structures

The GaAs-AlGaAs CTD structures were grown by molecular beam epitaxy at Georgia Tech. Full two inch, n+ GaAs substrates were used, and were mounted using In-free substrate holders to minimize surface defects and subsequent backside processing. The second and third CTD process runs were performed on MBE Run ID B92-88, which had the

material structure listed in Table 3.2.

A schematic of the process flow for the CTD structure is shown in Figure 3.3. Mesa isolation was performed with a phosphoric acid based etchant. The mesa etch depth was 0.41μm, which isolated the readout and top well barrier layers from the remainder of the structure.

Ion implantation was used to form the overflow junction, a p-type ring around the charge storage well which can be used to bleed excess charge from the storage well. The photoresist used previously to define the mesas was left on the wafer to act as the ion implantation mask. The ion implantation was performed at Implant Sciences. The conditions for the four Be^+ implants are shown in Table 3.3.

The implant profiles were computed using the "Profile Code" software provided by Implant Sciences, with the summation profile of the four individual implants profiles shown in Figure 3.4. The implants should yield a highly doped ($\sim 2x10^{18}$ cm^{-3}) surface layer for facilitating low resistance ohmic contacts to the overflow barrier, which consists of a lower doped ($\sim 1x10^{17}$ cm^{-3}) region that extends down to a depth of 0.4μm. The resultant two-dimensional CTD material structure is shown in Figure 3.5, with the vertical direction drawn to scale.

After ion implantation, the 2" wafer was divided into quarters for use in the second and third CTD process runs. The process flow for both fabrication runs was identical to that shown in Figure 3.3. However, the implementation of the implant activation annealing step differed between the two process runs, and will be described subsequently.

The next process step for CTD fabrication was a high temperature thermal anneal,

Table 3.2 Material Structure for MBE Run B92-88.

Designation	Material	Thickness (μm)	Doping Density (cm^{-3})
Readout	GaAs	0.2	$n = 1x10^{17}$
Top Well Barrier	GaAs	0.2	$p = 6x10^{16}$
Charge Storage Well	GaAs	0.2	$n = 6x10^{16}$
Bottom Well Barrier	$Al_{0.45}Ga_{0.55}As$	0.1	undoped
Grading Layer	$Al_{0.45}Ga_{0.55}As$ graded to GaAs	0.15	$n = 2x10^{18}$
Substrate	GaAs	NA	$2x10^{18}$

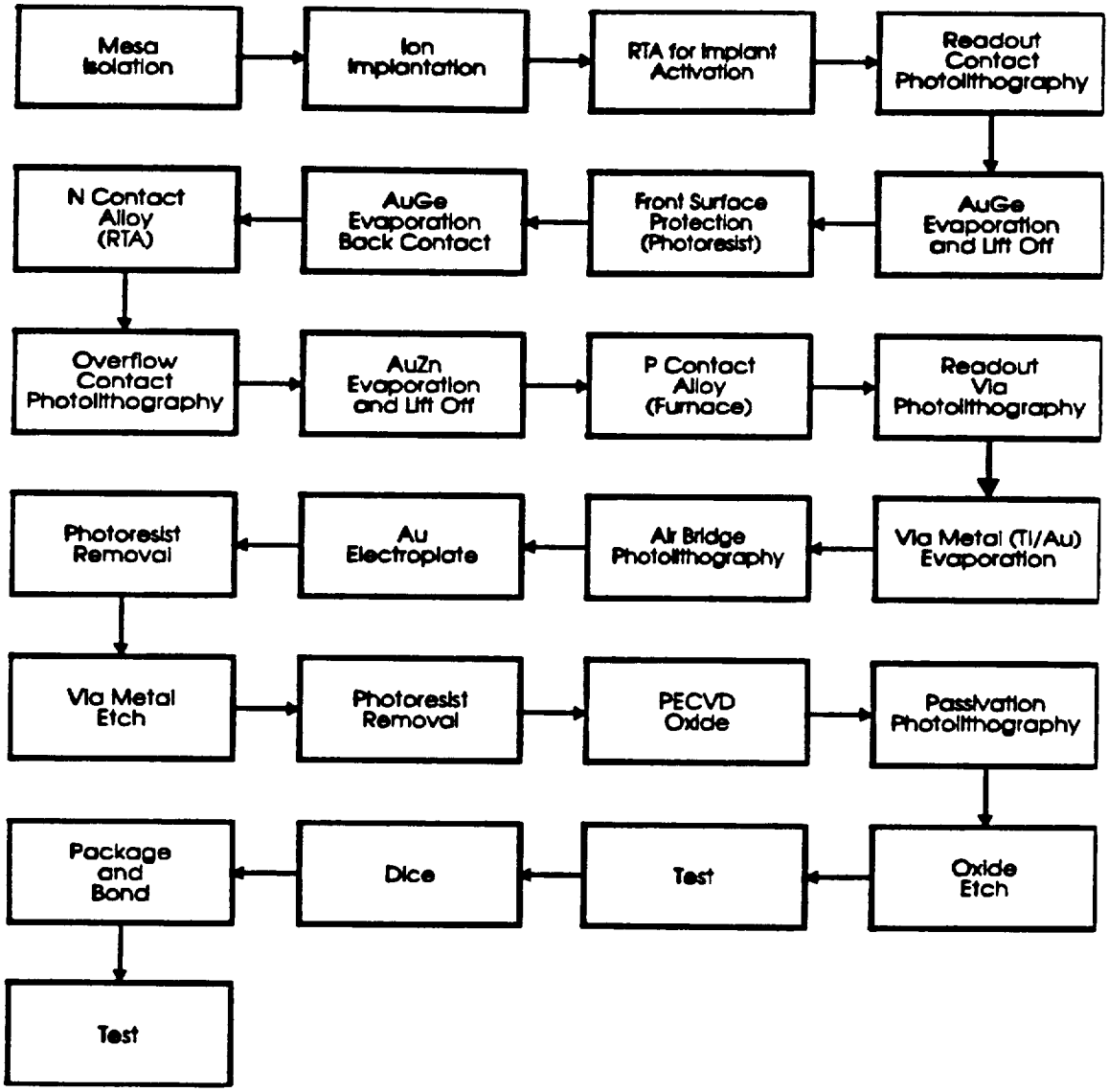


Figure 3.3 Schematic of the CTD fabrication process.

Table 3.3 Ion Implant Conditions for B92-88.

Implant Energy (keV)	Dose (cm^{-2})
145	$3.69x10^{12}$
70	$1.25x10^{12}$
30	$9.55x10^{11}$
7	$1.00x10^{13}$

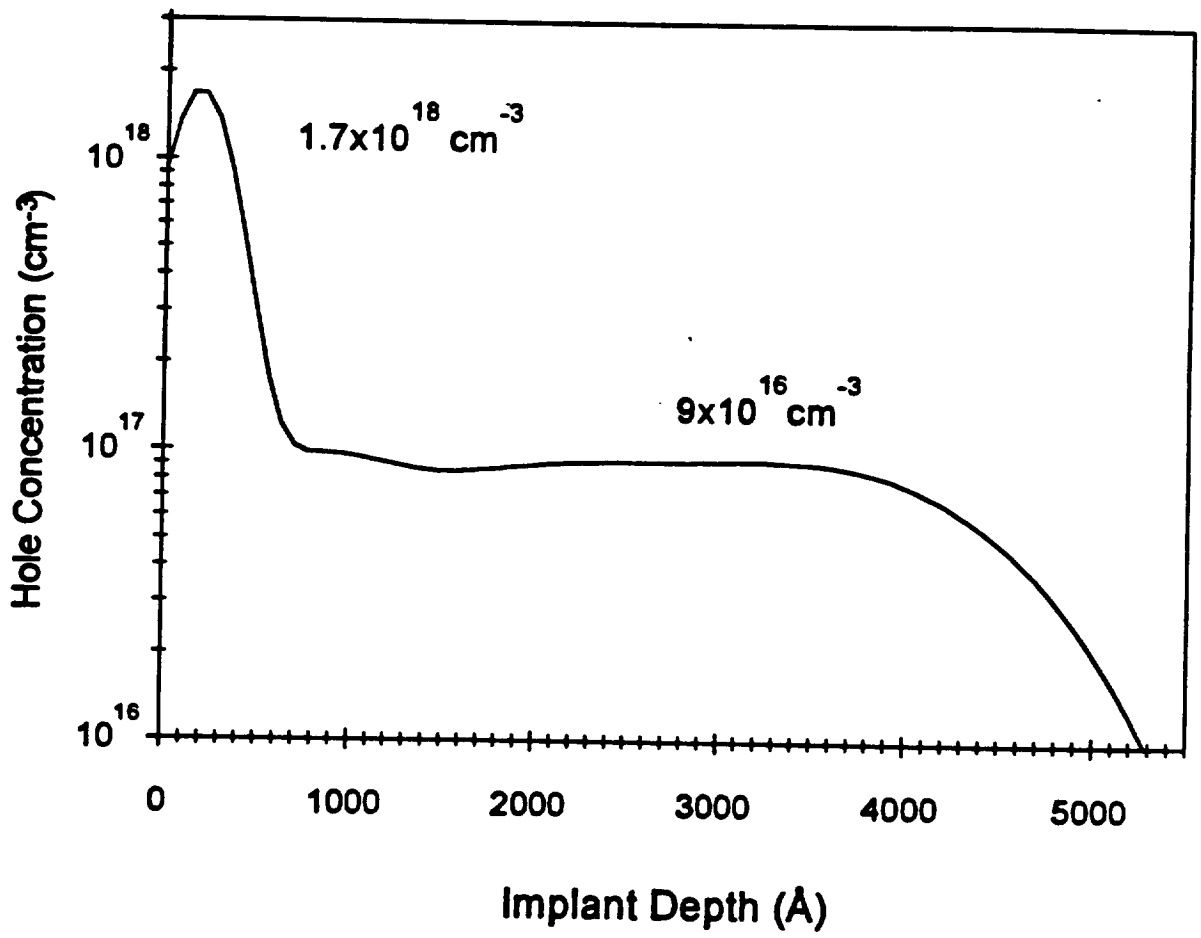


Figure 3.4 **Computed ion implant profile for CTD structure on MBE run ID B92-88.**

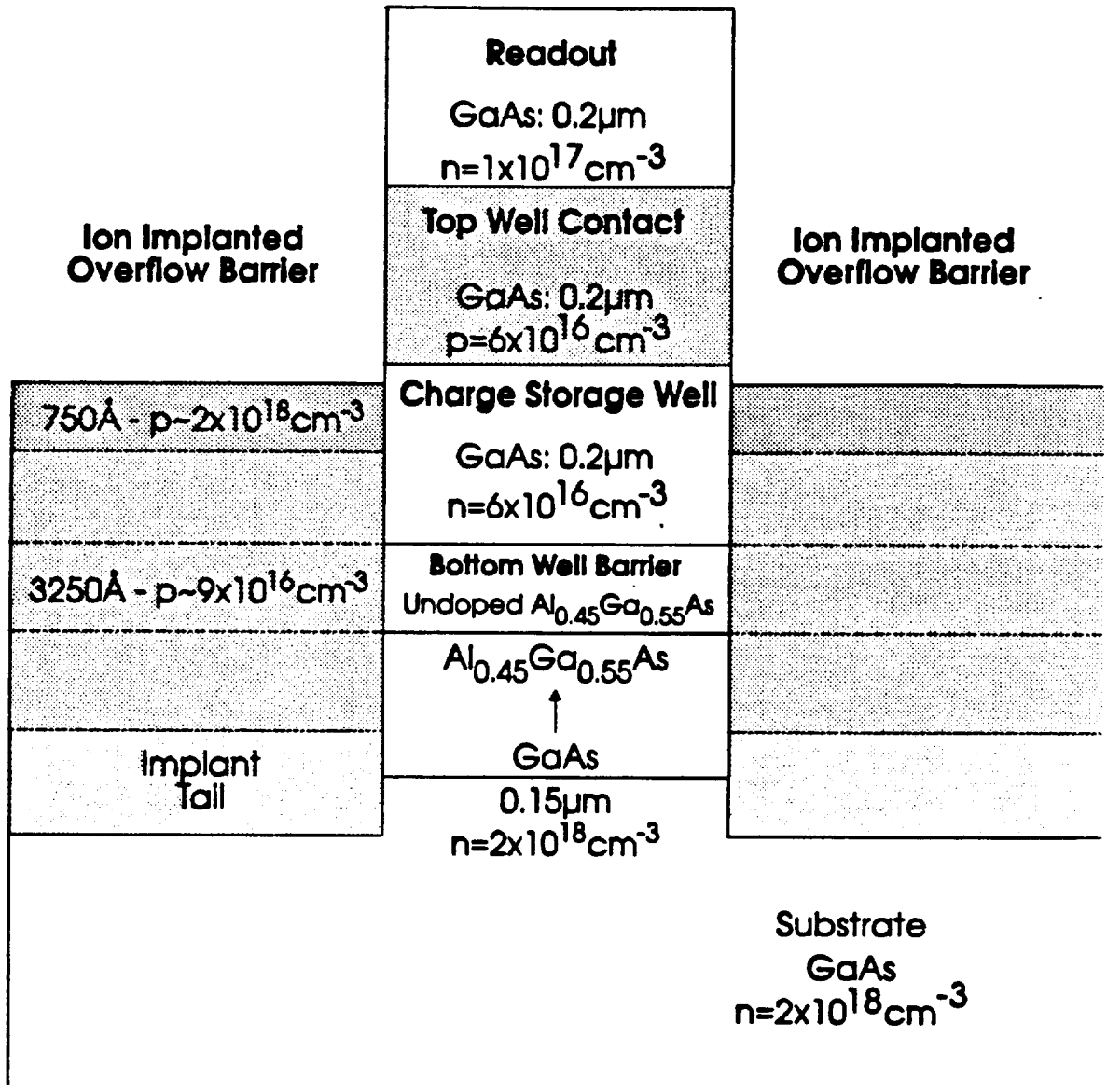


Figure 3.5 **Schematic of two-dimensional material structure for processed CTD, with the vertical direction to scale.**

which was required to activate the Be dopant atoms and to remove crystal damage from the implant. A rapid thermal processor (RTP) was used for this implant activation annealing step, as described in the previous report. For successful rapid thermal annealing (RTA) of GaAs, a critical process goal is to minimize the loss of high vapor pressure As from the surface. Arsenic loss causes severe surface degradation, which is unexceptable for device photolithography, and also introduces electrically active point defects (i.e. vacancies) into the GaAs.

To prevent As loss from the surface, the GaAs surface is physically capped before high temperature annealing. There are two general capping technologies used for GaAs processing. The first technology is based on proximity capping, which uses an As source (such as a GaAs wafer) in intimate contact with the GaAs material to be annealed. The second capping technology uses a deposited thin film, typically Si_3N_4 (nitride) or SiO_2, to prevent As loss from the surface. The implant activation experiments described in the first report used proximity capping. Although proximity capping yielded high dopant activation and negligible surface degradation under optimum operating conditions, the implementation of that technique suffered from poor reproducibility, in the form of localized areas with surface degradation. This effect resulted from imperfect wafer-cap contact, especially when the technique was used with larger pieces (i.e. wafers). The cause of this problem is difficult to isolate, but must be related to the thermal geometry of the RTP susceptor.

Therefore, for RTA of the overflow ion implant, it was decided to use a nitride cap layer for the second CTD process run. The nitride was deposited by PECVD in a PlasmaTherm 700 series system, with the detailed deposition parameters given in the

previous report. Initial tests of the nitride cap during typical ion implant activation RTA (800-900°C) showed large scale blistering of the nitride cap, with resultant GaAs surface degradation from As loss. Figure 3.6 shows a photomicrograph of a blistered GaAs surface after removal of the nitride in an HF solution. From this figure it is apparent that these blistered surface were not suitable for GaAs CTD fabrication.

Discussions with PlasmaTherm identified the cause of blistering as explosive loss of volatile materials such as oxygen or hydrogen from the GaAs surface through the nitride cap. This volatile contamination resulted from incomplete removal of organics such as photoresist or solvents from the surface, and from the presence of a surface oxide layer on the GaAs. The surface oxide layer was formed during ambient exposure before introduction to the PECVD system and also at an accelerated rate during loading of the GaAs into the PECVD system, as a result of the PECVD platen being maintained at 300°C during loading to achieve maximum system throughput. These operating conditions are routinely used with the PECVD system because it is commonly used for Si processing, where oxide formation is not detrimental. A final difficulty with the operation of the PECVD system was that the deposited material in the chamber adsorbed water vapor from the ambient during sample loading, which then caused oxygen contamination of the nitride. This contamination resulted in a less robust nitride which blistered easier under thermal stress. These problems were not appreciated previously when processing Si, because the nitride coatings were not subjected to high temperatures or volatile surface layers.

After identifying these causes of nitride blistering, a new cleaning and loading procedure before nitride deposition was developed, with a goal of minimizing GaAs oxide

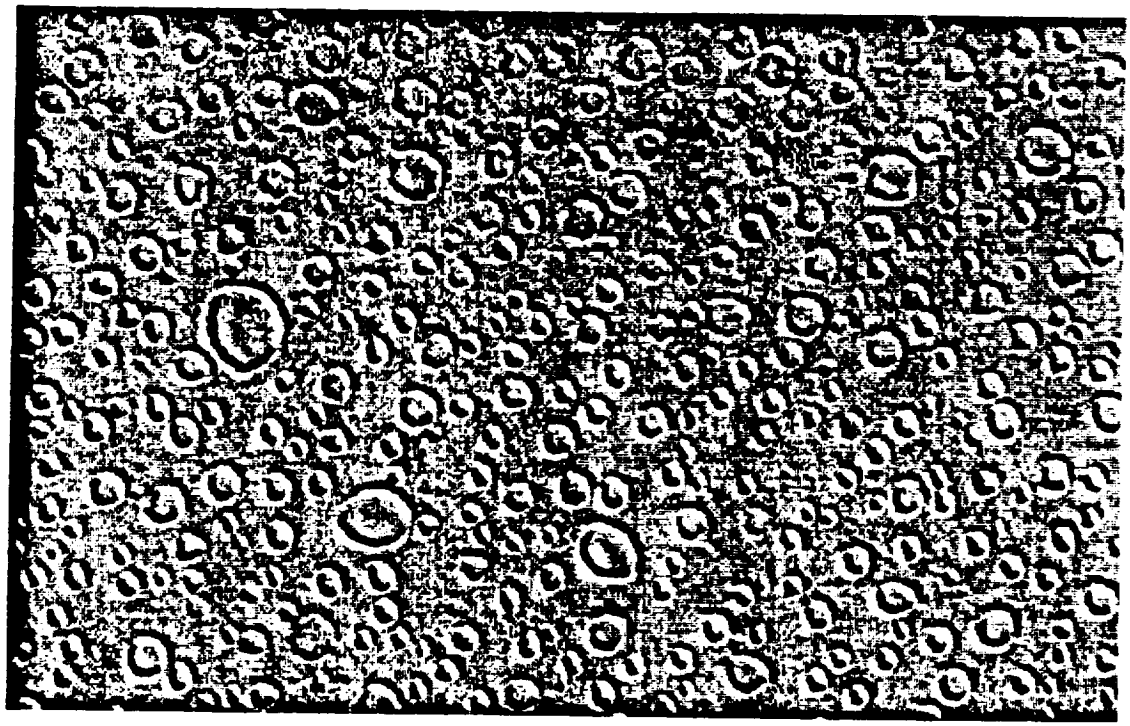


Figure 3.6 **GaAs surface after RTA with nitride cap. Surface displays blistering.**

formation: The GaAs surface oxide was chemically removed immediately before loading into the PECVD system. Oxide removal was by a concentrated HCl etch to remove oxides and a 1:1 NH_4OH-water solution to remove excess surface As [17].

To minimize GaAs oxidation during loading of the PECVD system, the platen was allowed to cool to 220°C before sample introduction. After sample loading the system was evacuated to a pressure of less than 10mTorr. Also, to minimize oxygen induced weakening of the nitride cap, the PECVD system was thoroughly cleaned before GaAs loading to remove all deposited material.

The RTA process for activating the overflow implants in the second CTD process run is comprised of two temperature steps. The process started at room temperature, with a temperature ramp of 30°C/s to 300°C for 10s. This low temperature step was incorporated to properly seat the sample on the susceptor in an attempt to minimize thermal stresses. The sample temperature was then ramped at 55°C/s to 850° for 10s to activate the implant. This choice of temperature-time product was based on experimental results that were described in the previous report, and should result in maximum activation of the overflow implant. After the activation RTA, the nitride was removed with a concentrated HF solution.

The new cleaning and loading procedure yielded nitride capping layers which showed reduced GaAs blistering during RTA. However, it was judged that the small amount of blistering present was not acceptable for the CTD's. The residual blistering was believed to result from the loss of film adhesion due to compressive stress in the PECVD nitride layer. Although this stress can be minimized through proper choice of deposition conditions, it was felt that much time would have to be invested to find the optimum deposition conditions,

given the large number of experimental variables in PECVD. Even if the compressive strain was minimized, the difference in thermal expansion coefficients between the nitride cap and the GaAs layer can introduce crystallographic defects into the GaAs. Another problem with nitride capping which may eventually become a concern for CTD fabrication is the diffusion of hydrogen from the PECVD nitride layer into the GaAs, where the hydrogen has been shown to passivate n-type dopants and possibly p-type dopants as well [18]. A final difficulty discovered during GaAs RTA, which was not unique to nitride capping, was the introduction of crystallographic slip defects into the wafer edges. This problem resulted from thermal stresses introduced into the GaAs from temperature gradients across the sample.

From the previous discussion, the optimum RTA process should utilize a properly designed proximity capping technique coupled with a uniform temperature distribution across the sample so as to prevent slip formation. This goal was realized through the construction of a specially designed proximity capping fixture for GaAs RTA. The fixture was annulus shaped and constructed of high purity, refractory molybdenum. At the ends of the fixture two 2" GaAs wafer caps, were included as the As source. The combination of fixture and GaAs cap wafers formed a sealed, arsenic rich environment in which the sample was placed, face up. Therefore, no damage occurred to the front surface as was possible during the previous implementation of proximity capping. The separation between the front surface of the sample and the top cap GaAs wafer was 0.050", and thus gave sufficient arsenic flux on the surface to prevent degradation.

To provide the uniform temperature environment necessary for slip-free GaAs RTA,

the combination fixture-GaAs cap wafers enclosure was specially treated to yield a constant temperature, blackbody environment. This goal was accomplished by increasing the emissivity of the inside surfaces by bead-blasting the inside of the molybdenum fixture. The surfaces of the GaAs cap wafers were also roughened by a short dip in concentrated nitric acid.

Testing of the new proximity capping technique yielded excellent results. No surface degradation or slip formation was observed for anneal temperatures of 1000°C and ramping rates of 100°C/s. Multiple high temperature anneals were possible without changing the GaAs cap wafers, although after 2-3 runs the surfaces were regenerated by concentrated nitric acid treatment.

The new proximity capping technique was used for the implant activation anneal in the third CTD process run. In addition, the temperature-time cycle was changed slightly as a result of new information found on the thermal activation of Be implants [19]. The new RTA cycle was essentially the same as for the second CTD process run, but included a 60s anneal at 650°C immediately after the short, 850°C activation anneal step. This longer, lower temperature step was incorporated to heal crystal defects without causing the anomalous Be diffusion observed at higher temperatures. Inspection of the sample surface after RTA showed no observable degradation, thus demonstrating the superiority of this new technique compared to the previous nitride capping layer.

Following p-type implant activation in both of the CTD runs, photolithography for the readout ohmic contact was performed, followed by AuGe/Ni/Au evaporation and lift off (refer to Figure 3.3). The front surface was then protected by a 4-5μm thick photoresist

layer, and an n-type ohmic contact metallization of AuGe/Ni/Au evaporated onto the back of the wafer. Both n-type contacts were then given an RTA at 365°C for 30s to reduce the contact resistance [20]. The overflow contact photolithography was then performed, followed by p-type ohmic metallization using AuZn/Au and lift off. The p-type ohmic metallization was furnace annealed at 400°C for 2min to reduce the contact resistance.

The process for formation of the air bridge used to connect the readout bonding pad to the readout ohmic contact was described in detail in the previous report. Figure 3.7 shows an SEM micrograph of a completed air bridge structure crossing over the overflow contact of a 40μm CTD. The excess metal visible in the foreground resulted from poor lift off of the Ti/Au via metallization (process modifications have been implemented to prevent reoccurrence). Figure 3.8 shows a completed cell of four CTD's of 40,20,10, and 8μm diameter.

The I-V characteristics of the completed CTD structures were probed to insure that the devices operated properly. Selected CTD's were then diced from the wafer using a Micro Automation 1006 dicing saw and packaged for C-V and current injection measurements.

3.2.2 Enhancements to Current CTD Fabrication Process

After successful completion of three CTD process runs, enhancements have been identified for the fabrication process. These enhancements are listed below and will be implemented through a new mask set for subsequent CTD process runs:

The mesa isolation depth will be increased so as to insure complete isolation between the top well barrier and the overflow barrier (see Figure 3.5). To prevent any effects from

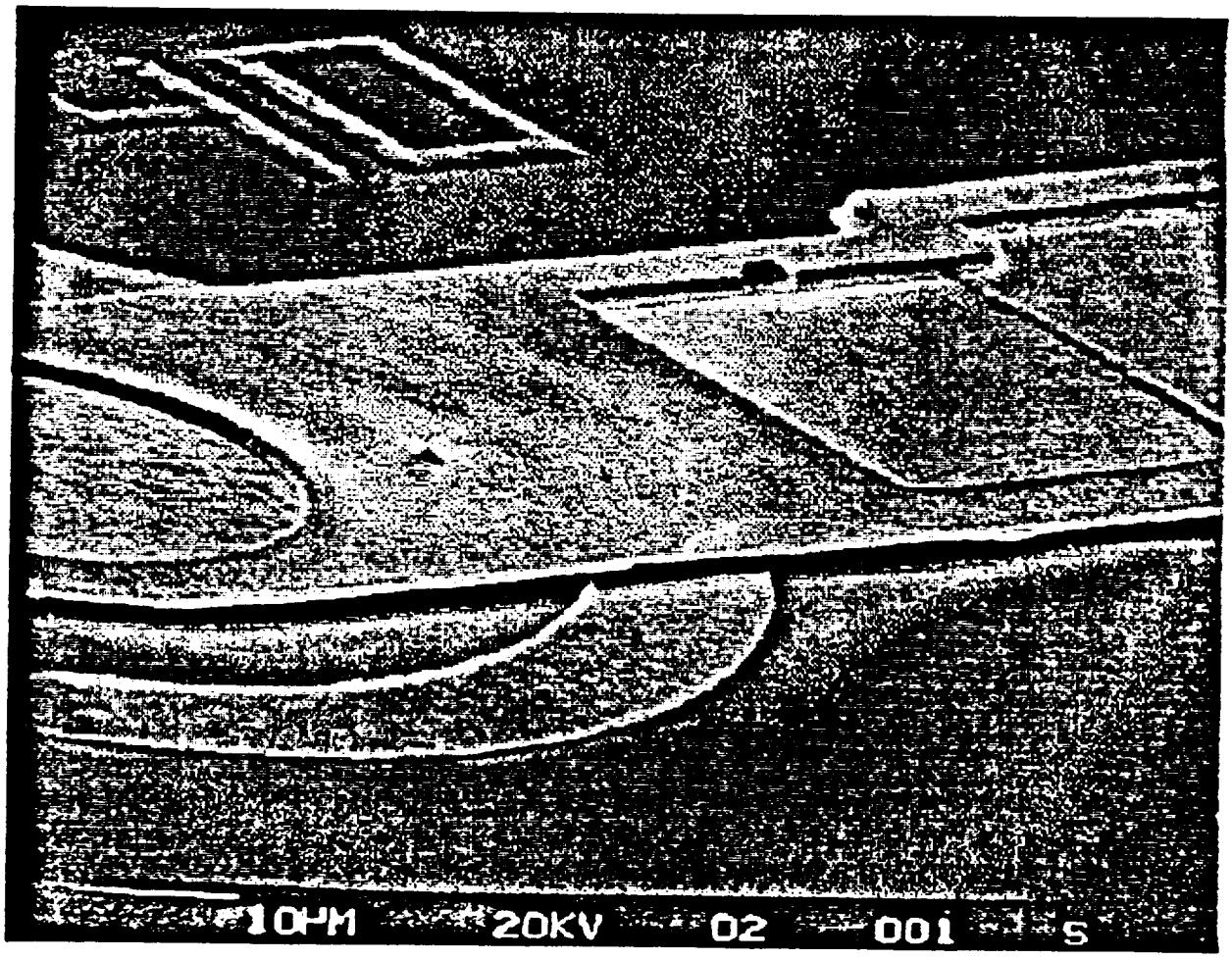


Figure 3.7 SEM micrograph of completed air bridge structure on 40μm CTD.

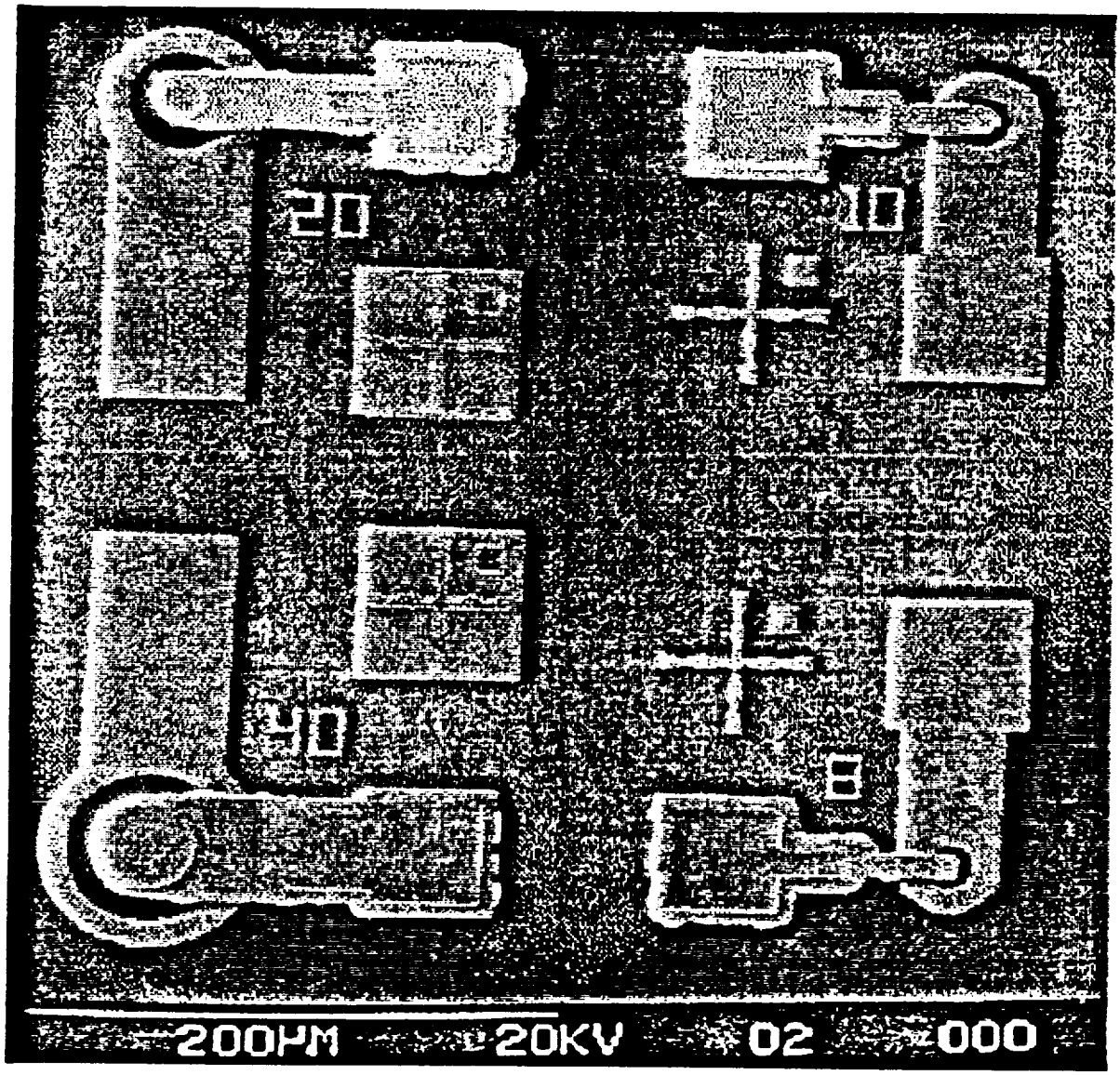


Figure 3.8 Completed cell of four CTD's of 40, 20, 10, and 8 μm diameter.

electrical shorting between these areas as a result of ion implantation, an additional photolithography step has been added to isolate the overflow implant from the walls of the mesa. In addition, this so-called implant protect mask will allow the use of a more process compatible photoresist for mesa definition.

The p-type ohmic contact process will now be performed before the n-type ohmic process, because of the higher temperature used in the p-type anneal which could possibly affect the n-type ohmic contact resistance. Another possible solution is the development of a lower temperature RTA process for the p-type ohmics.

Test structures have been added to the mask set to allow evaluation of the specific contact resistance of the n- and p-ohmic contacts. Schottky diode devices and FETs will also be incorporated for dopant profiling and mobility evaluation of the implanted regions.

The mask set has been modified to allow gold electroplating of the p-type ohmic overflow contacts. This change will result in easier gold wire bonding to these pads.

The carrier concentration for each wafer will be determined by electrochemical capacitance-voltage profiling to insure the required material doping structure. In addition, an area at the edge of the wafer will be processed for electrochemical and SIMS dopant profiling of the ion implant profile after activation.

3.2.3 Characterization of Charge Transfer Device

As described previously the charge transfer device (CTD) serves to store charge accumulated from an avalanche photodiode (APD), bleed off excess charge to prevent pixel blooming, and to transfer the stored charge to the acoustic charge transport (ACT) region for pixel readout. The current structure under evaluation is diagrammed in Figure 3.9. The

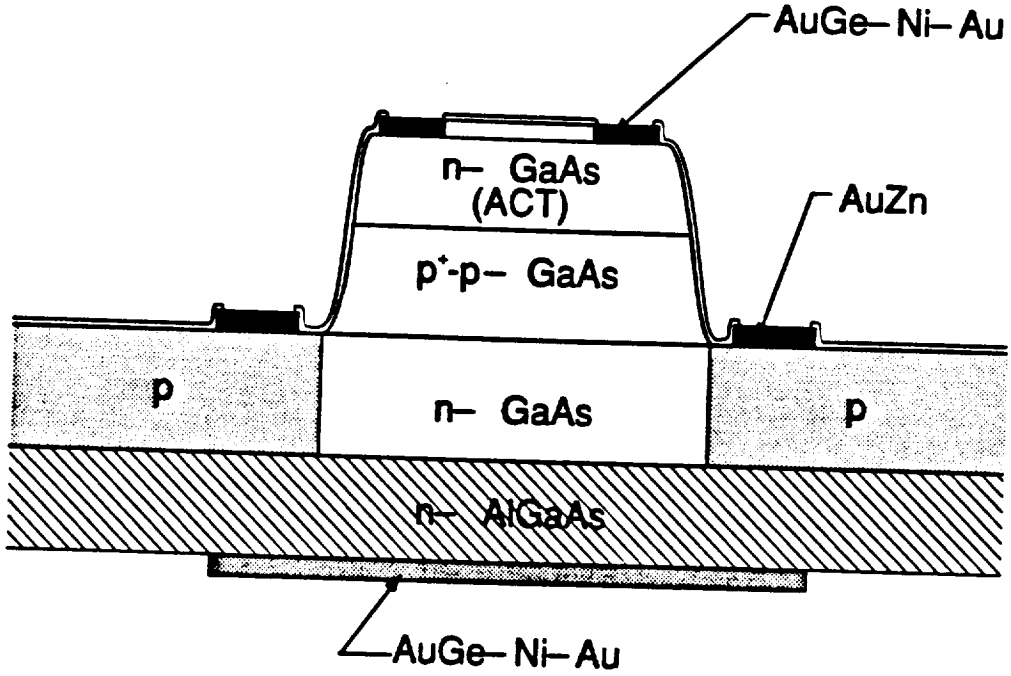


Figure 3.9 Cross-sectional view of charge transfer device.

bottom AlGaAs layer is the end of the n-type region of the p-i-n APD. This layer is separated by a thin intrinsic AlGaAs layer from the n-type GaAs well region. This region acts as a potential well for electrons because it is bounded on the sides and above by p-type GaAs and below by the larger bandgap AlGaAs. The p-type GaAs surrounding the well acts as an overflow contact by allowing excess electrons to "spill" out of well. The overflow barrier height can be adjusted by a combination of external bias and the doping levels in the overflow and well regions. The well is bounded above by p-type GaAs which is capped by an n-type GaAs layer, corresponding to the ACT channel region. The well barrier in this direction can also be adjusted through doping levels and p-type region thickness.

The device basically operates as follows. The APD injects electrons across the AlGaAs barrier and into the well. Here the charge accumulates until the p-type layer barrier above it is lowered and the charge pulled out. In order to accomplish this, a readout bias must be applied to first breakdown the top n-p junction and then to pull the stored electrons through the forward biased p-n junction. This operation must be accomplished in conjunction with the passage of a surface acoustic wave to sweep the charge away. However, if too much charge accumulates between read outs, the excess will be drained away through the overflow contact.

An analysis of the structure indicates that the three main functions of the CTD (charge storage, overflow and readout) are interdependent and must, therefore, be well controlled and characterized. Characterization of each of these functions is currently underway. The test equipment currently utilized for these measurements or which is in the process of being obtained is as follows.

Tektronix DSA602 Digital Storage Oscilloscope

Tektronix AWG2020 Arbitrary Waveform Generator

HP4280A Capacitance Meter

HP4277A LCZ Meter

HP4145B Semiconductor Parameter Analyzer

Keithley 224 Programmable Current Source

3.2.3.1 Initial Measurements

Before any measurements were undertaken, devices were chosen in contiguous groups of three from various locations on the processed wafer and were probed at an I-V station to ensure that there were no open circuit devices. Next, the device groups were sawed from the wafer and mounted in a 8 pin DIP package. The devices were then bonded in such a manner as to permit isolated connections to each of the devices.

Initial current-voltage measurements using the parameter analyzer indicate that:

1. a relatively high bias must be applied to the back AlGaAs and top n-GaAs contacts to conduct any current (the overflow contact is floating)
2. applying a bias to the overflow contact allows conduction through the overflow and top contact at lower biases
3. samples initially exhibit "back to back" diode type I-V (soft turn-ons)

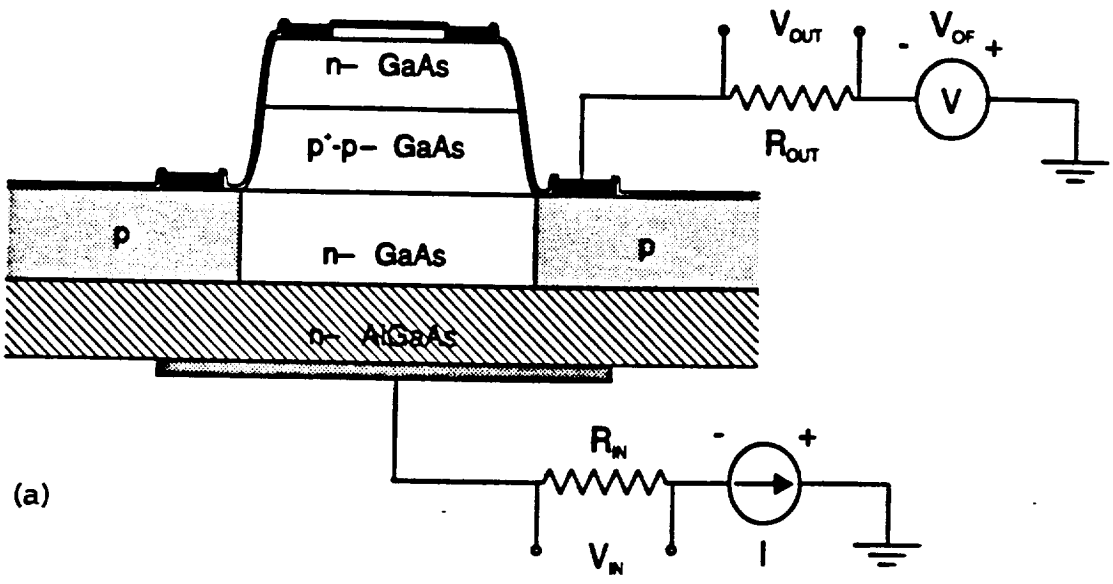
3.2.3.2 Overflow/Storage Capacity Characterization

This aspect of the CTD characterization will involve the determination of the well charge storage capacity as a function of the bias on the overflow contact (V_{OF}). As mentioned previously, V_{OF} will affect the overflow barrier height and, thus, the well

capacity. Another effect which will be investigated is the forward biasing of the n(well)-p(overflow) junction as charge accumulates in the well. In fact, by adjusting the doping levels, it may be possible to have a self-regulating overflow mechanism. Schematic and block diagrams of the basic circuit are presented in Figures 3.10a and b, where the subscripts OF, OUT and IN refer to overflow, output and input, respectively. The two curves in Figure 3.11 qualitatively show the predicted behavior of I_{IN} and I_{OUT}. A constant current source (I_{IN}), which turns on at t=0, is used to fill the well with charge. Eventually, the well overflow junction will be forward biased enough to start conducting charge. At this point, the amount of charge transferred into the will is equivalent to the capacity of the well for that particular doping level and V_{OF}. The charge capacity will be obtained by integrating the current from t=0 to the time at which the I_{OUT} starts to increase.

3.2.3.3 Storage Time Capacity

The next related device parameter to be characterized is the storage time of the CTD well. In combination with the storage capacity, this time will affect the signal integration and readout rate capabilities of the device. The simplified test circuit is illustrated in Figure 3.12a and a block diagram representation in Figure 3.12b. This circuit is similar to the one previously discussed except that V_{OF} is supplied by the internal bias supply of the Hewlett Packard capacitance meter. After applying current input pulses of varying lengths and magnitudes, the recovery of the capacitance is monitored. Although, the measured capacitance will not directly monitor the n(well)-p(overflow) junction, the time dependence should represent the change in the amount of charge stored in the well. The expected characteristics are shown in Figure 3.13. These measurements are being carried



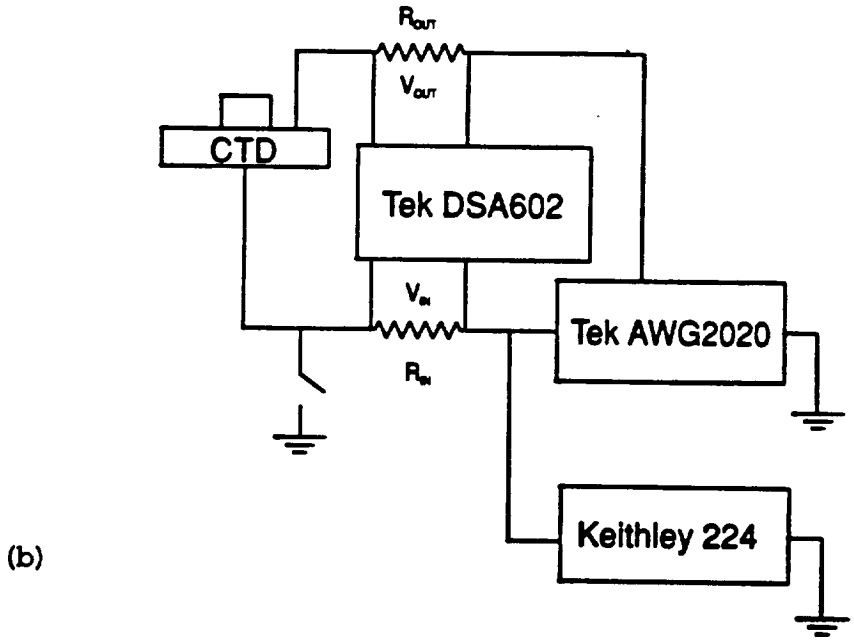


Figure 3.10 **Overflow/Storage capacity characterization a) schematic circuit and b) block diagram.**

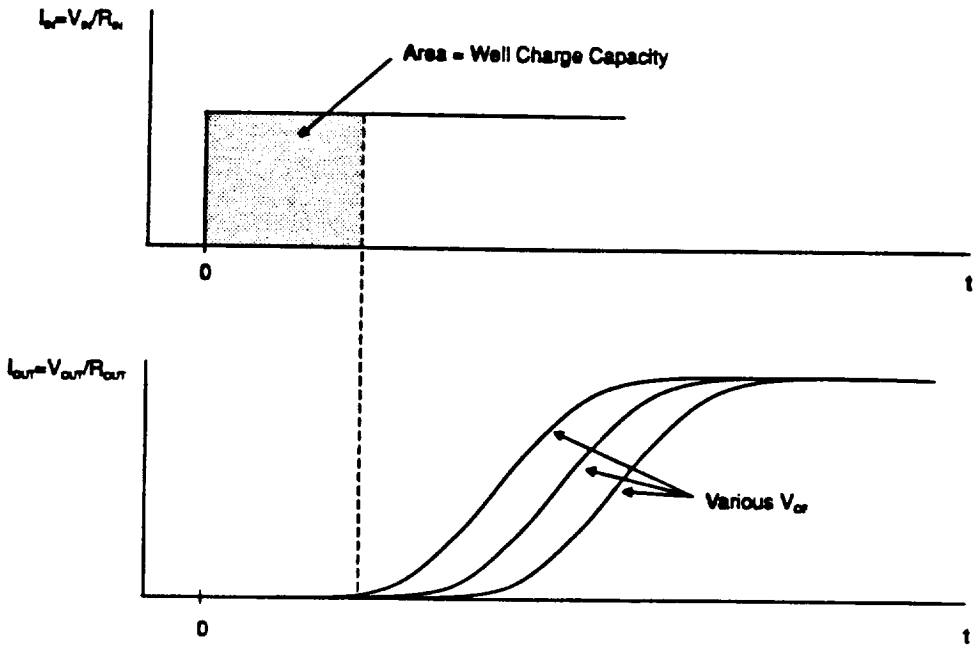


Figure 3.11 Predicted behavior of overflow/storage capacity circuit.

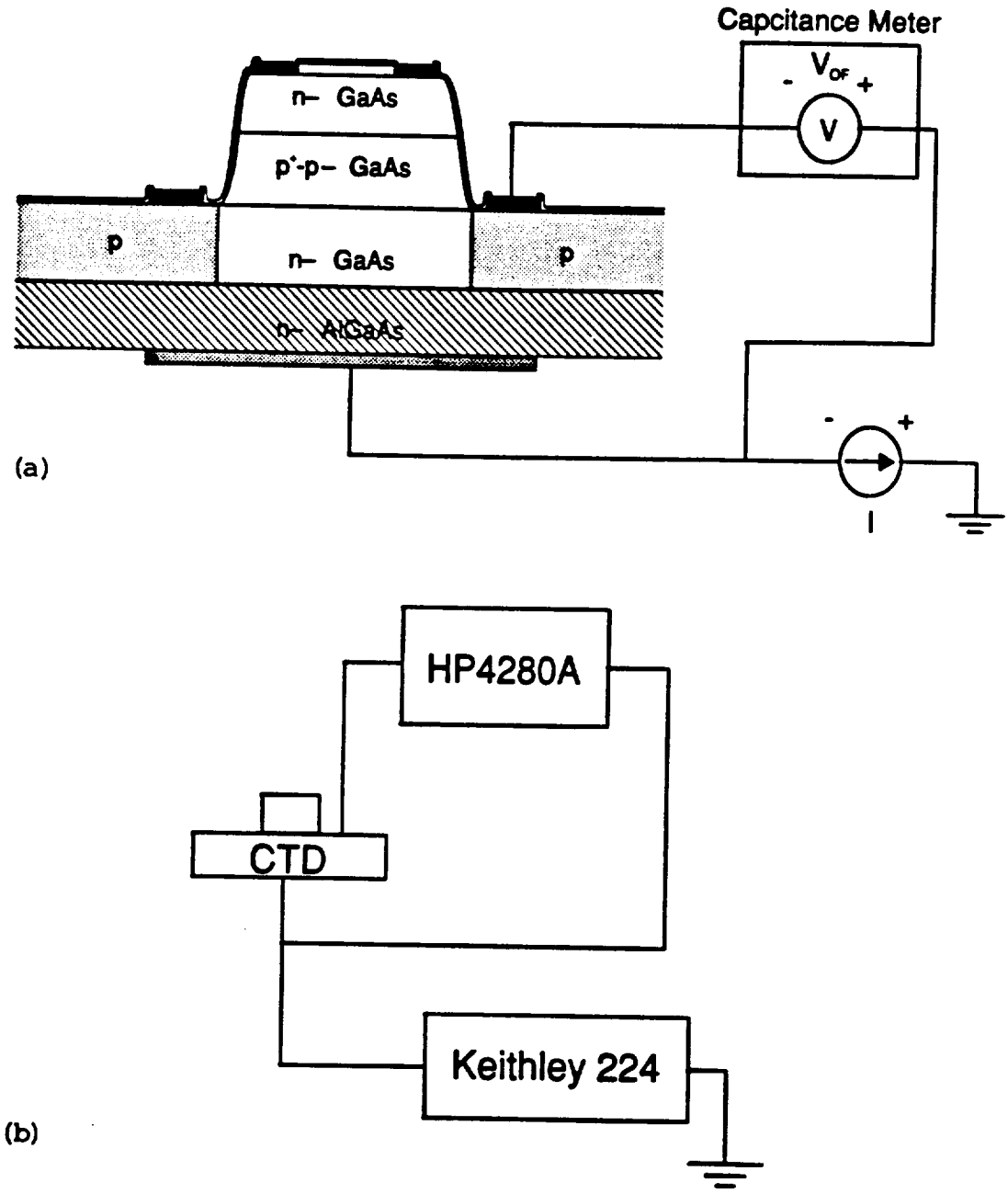


Figure 3.12 Storage time characterization circuit a) schematic and b) block diagram.

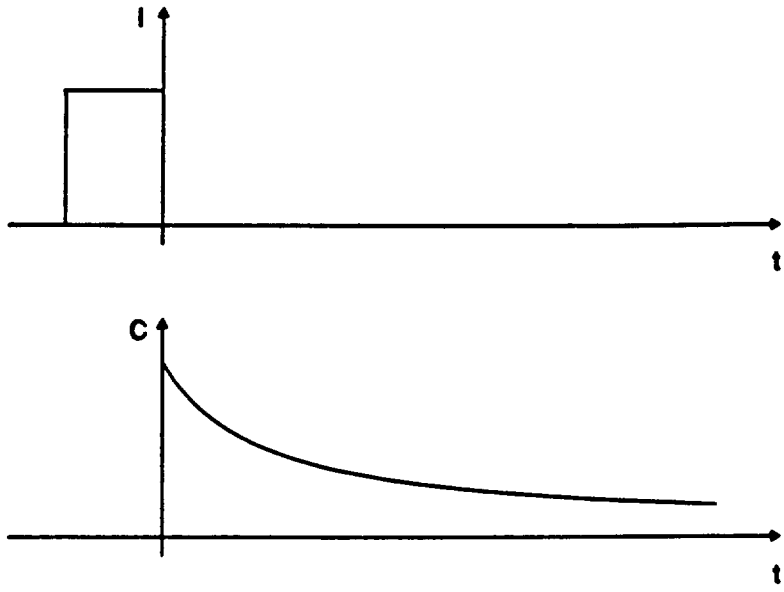
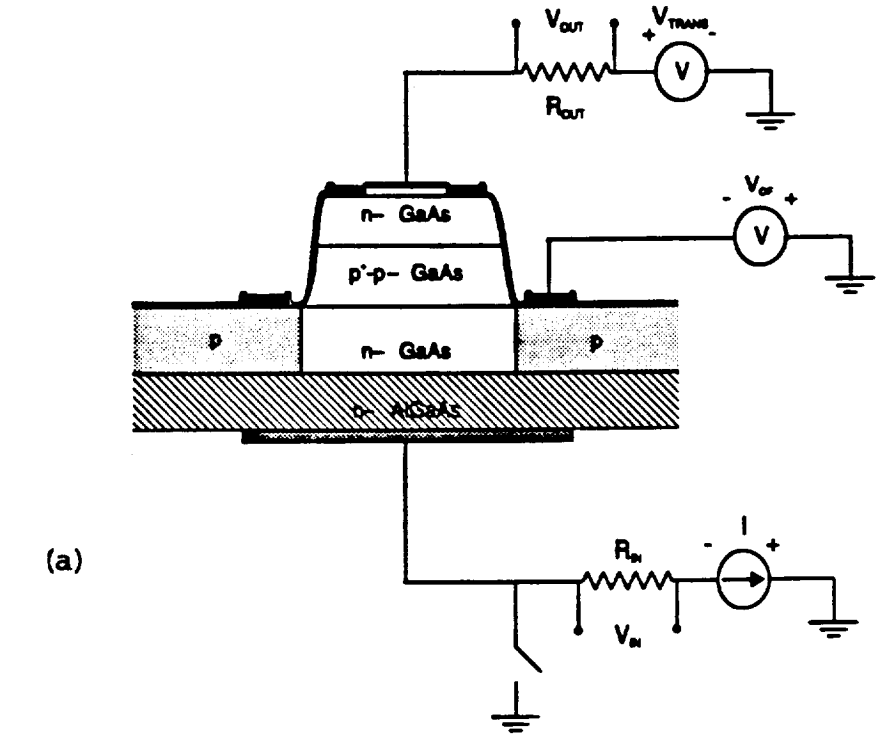


Figure 3.13 The expected characteristic of the storage time circuit.

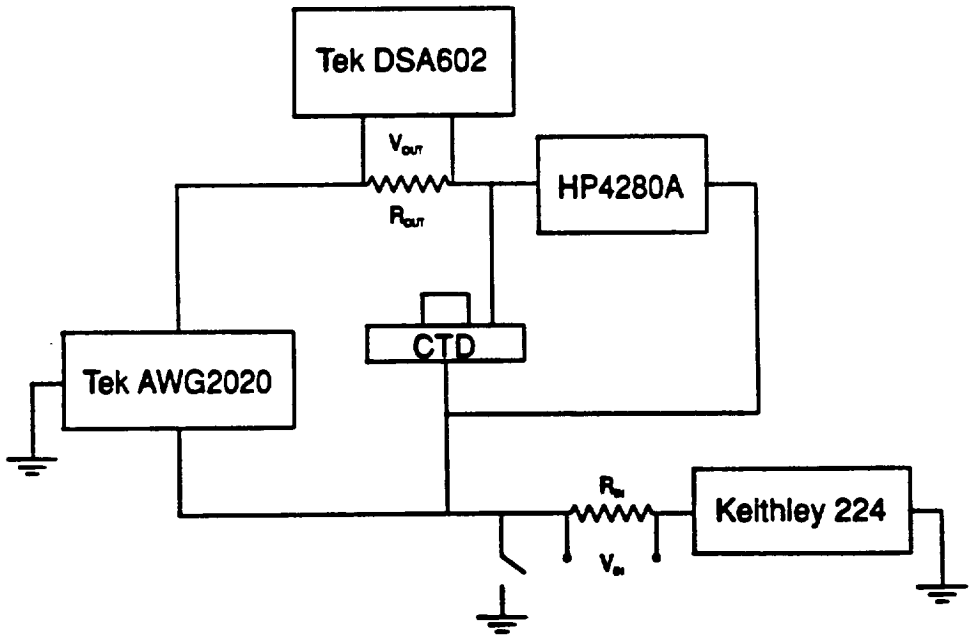
out as a function of V_{OF}.

3.2.3.4 Efficiency of Charge Transfer

The characterization of the charge transfer efficiency will be accomplished as follows. The well will be first filled to capacity for a specified overflow contact bias and the back AlGaAs contact grounded. A positive bias will then be applied to the readout contact to first breakdown the n(ACT region)-p(well barrier) junction and to pull the charge out of the well. However, since the charge in the well will tend to forward bias the barrier between the well and the ACT region, it is possible that the turn-on bias for charge transfer will vary as the charge is drawn out of the well and also with the initial amount of charge stored in the well. Figures 3.14a and b show a schematic and block diagram of the circuit utilized for this characterization. First a well filling pulse is applied (I_{IN}), as determined from the previous charge storage measurements. Next, a readout voltage (V_{TRANS}) consisting of a d.c offset and a rectangular pulse is applied and V_{OUT} monitored as a function of time to determine the threshold voltage necessary to transfer the charge for the specified conditions. The V_{OUT} waveform will be integrated to give (in combination with the previous storage capacity measurements) the amount of charge transferred and the efficiency of the transfer as a function of readout pulse width and magnitude. Trapezoidal readout pulses will also be investigated to study the effect of the amount of stored charge upon the required readout bias. As the transfer bias is increased, it is expected that the AlGaAs junction will start conducting or perhaps the overflow junction will breakdown (depending upon V_{OF}, etc.). The expected characterization waveforms are shown in Figure 3.15.



(a)



(b)

Figure 3.14 **Charge transfer efficiency characterization circuit a) schematic and b) block diagram.**

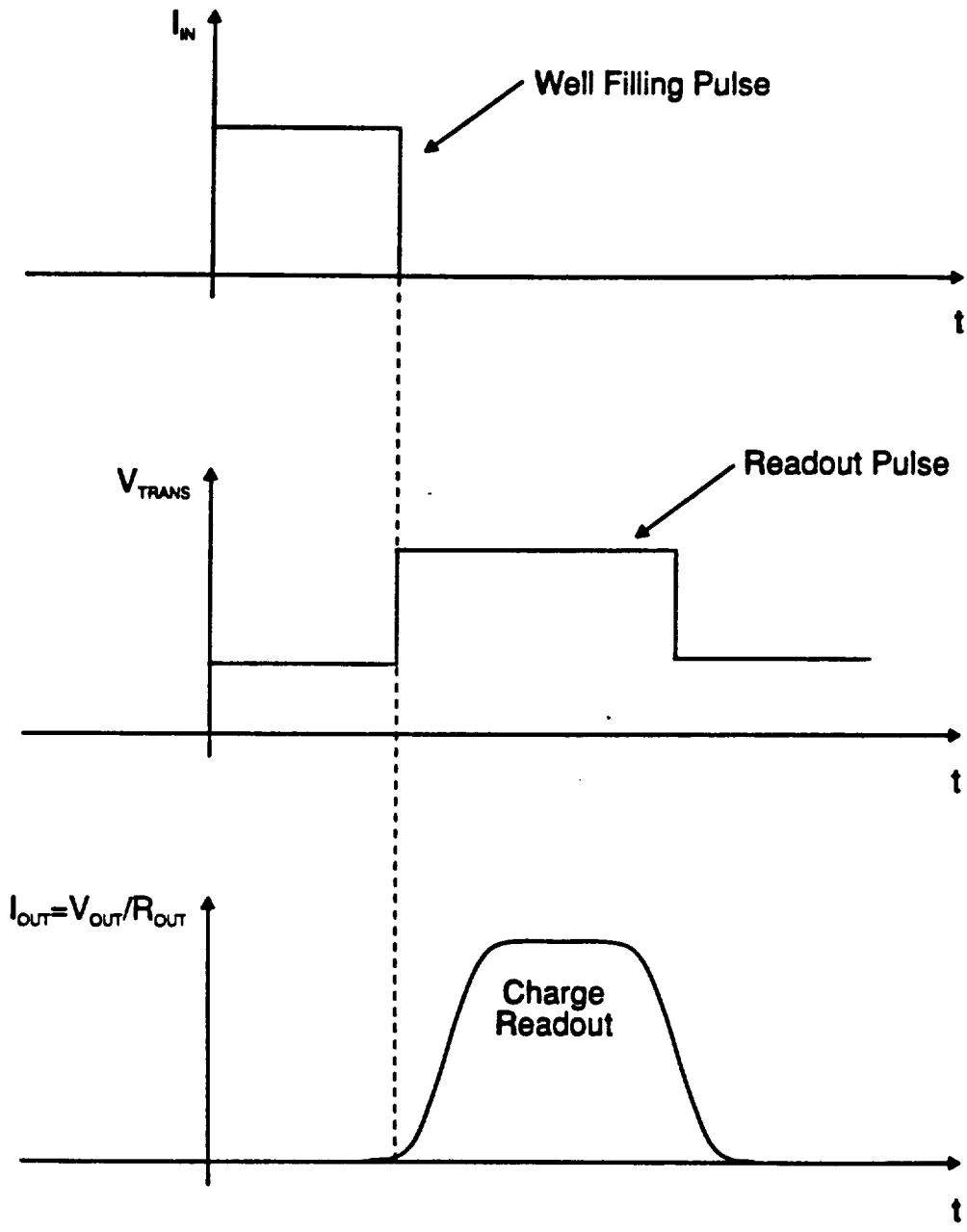


Figure 3.15 The expected response waveforms of the charge transfer circuit.

3.3 Material Growth Program

During this period a variety of structures were grown for HACT, CTD and SLAPD applications. Table 3.4 lists the samples grown for these applications.

3.3.1 Growth of Particle Free Surfaces

Studies were continued to minimize surface defects, such as oval defects and to minimize particulate contamination in order to obtain large area defect free material.

Two improvements were made to the Ga source to eliminate oval defects. First a dual zone Ga furnace, which has a second heater filament near the lip of the crucible, was substituted for the original furnace. This allows the lip of the crucible to be heated to a higher temperature than the rest of the cell thus avoiding Ga droplet formation near the lip. Secondly, we have purchased a new crucible made of pyrolitic boron nitrite (PBN) and pyrolitic graphite (PG). The base of the crucible is made of PBN as before, but the crucible lip has a thin layer of high thermal conductivity PG sandwiched between two PBN layers. Therefore, the crucible lip can be uniformly heated to a higher temperature, hence avoiding Ga droplet formation and oval defect formation. In samples grown using this source no oval defect formation was observed.

To minimize surface contamination a special glove box was designed and built. The box was made of glass and stainless steel and equipped with HEPA filters and an ionizer bar to achieve a class 10 environment. The box is directly interfaced with the load lock entry chamber of the MBE system to reduce particle contamination during the sample mounting and loading process. Since this chamber has been in full operation, the average defect count has been significantly decreased. New substrate mounting techniques have also been devised

Table 3.4. A list of samples grown.

RUN #	STRUCTURE	SURFACE PARTICLE DENSITY cm^{-2}
B92-65	HACT $n=2*10^{17}cm^{-3}$	
B92-65A	Doping Sample	
B92-66	Doping Sample	
B92-67	HACT $n=2*10^{17}cm^{-3}$	
B92-68	HACT $n=2*10^{17}cm^{-3}$	
B92-69	HACT $n=2*10^{17}cm^{-3}$	1445
B92-70	HACT $n=2*10^{17}cm^{-3}$	780
B92-71	HACT $n=2*10^{17}cm^{-3}$	554
B92-72	HACT $n=2*10^{17}cm^{-3}$	1364
B92-73	MWQ Structure	
B92-74	HACT $n=2*10^{17}cm^{-3}$	1872
B92-75	HACT $n=2*10^{17}cm^{-3}$	1415
B92-76	HACT $n=2*10^{17}cm^{-3}$	350
B92-77	HACT $n=2*10^{17}cm^{-3}$	1419
B92-79	MQW Structure	470
B92-80	HACT $n=2*10^{17}cm^{-3}$	920
B92-81	HACT $n=2*10^{17}cm^{-3}$	1255
B92-82	HACT $n=2*10^{17}cm^{-3}$	675
B92-83	HACT $n=2*10^{17}cm^{-3}$	819
B92-84	HACT $n=2*10^{17}cm^{-3}$	693
B92-86	CTD $p=6*10^{16}cm^{-3}$	949
B92-87	CTD $p=2*10^{17}cm^{-3}$	945
B92-88	CTD $p=6*10^{16}cm^{-3}$	497
B92-89	CTD $p=2*10^{17}cm^{-3}$	592
B92-90	HACT $n=2*10^{17}cm^{-3}$	
B92-91	HACT $n=2*10^{17}cm^{-3}$	
B92-92	HACT $n=2*10^{17}cm^{-3}$	

B92-93	HACT $n=2*10^{17}cm^{-3}$	675
B92-95	HACT $n=2*10^{17}cm^{-3}$	1075
B92-96	HACT $n=2*10^{17}cm^{-3}$	420
B92-97	HACT $n=2*10^{17}cm^{-3}$	
B92-98	HACT $n=2*10^{17}cm^{-3}$	682
B93-1	HACT $n=2*10^{17}cm^{-3}$	1793
B93-3	MQW Structure	1126
B93-4	MQW Structure	1830
B93-5	MQW structure	892
B93-6	HACT $n=2*10^{17}cm^{-3}$	
B93-7	HACT $n=2*10^{17}cm^{-3}$	1088
B93-8	HACT $n=2*10^{17}cm^{-3}$	691
B93-9	HACT $n=2*10^{17}cm^{-3}$	701
B93-13	MQW Structure	
B93-14	MQW Structure	
B93-17	MQW Structure	552
B93-18	MQW Structure	2369
B93-19	MQW Structure	915
B93-20	CTD $p=2*10^{17}cm^{-3}$	300
B93-21	CTD $p=2*10^{17}cm^{-3}$	176
B93-22	CTD $p-2*10^{17}cm^{-3}$	217

to minimize handling.

3.3.2 Indium Free Mounting

As discussed previously, MBE layers mounted with indium cause complications in the fabrication process. Furthermore, indium mounting causes extra wafer handling prior to growth and hence contributes significantly to surface contamination. However, the high thermal conductivity and ductility of In holds the wafer evenly, and equally disperses the heat across the wafer, thus producing a uniform temperature across the wafer.

One non-indium mounting technique involves clamping the wafer onto the molyblock. However, clamping causes unacceptable strain on the wafer during growth and reduces the heat transfer from the moly to the GaAs because the wafer is no longer in intimate contact with the substrate holder. Thus, the heat transfer to the wafer, occurs by direct radiation.

To obtain a strain free mount a spring loaded mechanism was first developed to clamp the substrate onto a moly ring using thin tantalum wire. However, a major disadvantage of this technique was that during mounting step the spring wire produced GaAs dust, which resulted in defective surfaces. This same mounting technique also placed the GaAs wafer in direct line of sight with the heating coils such that the substrate could be heated to 700°C. However, a significant temperature nonuniformity was observed because in the absence of the molyblock the thermocouple assembly was in close contact with the substrate and consequently produced a cooler central region, and temperature variations across the wafer. The heating station and thermocouple was therefore pulled back and fastened to prevent it from shielding the substrate. It is also clear that with this set up the

thermocouple can no longer accurately measure the surface temperature and thus a new temperature measurement scheme was required.

3.3.3 Temperature Measurement

When the substrate is radiatively heated, the thermocouple is not in intimate contact with the substrate and there is a large temperature difference between the thermocouple reading and the actual substrate temperature. Previously an IR pyrometer was used for remote sensing of surface temperature. This arrangement worked well for indium mounted wafers because the pyrometer employed a lead sulfide detector with a special notch filter from 2.1 μm to 2.5 μm (0.6 eV to 0.5 eV). The pyrometer thus sensed the temperature of the moly surface by looking through the GaAs wafer whose bandgap energy is between 1.42 eV and 1.21 eV for temperatures of 300 - 700°C. With no metal backing the GaAs wafer, the pyrometer will now only detect radiation from the heater filaments instead of the GaAs surface temperature and thus, is not suited for use with a direct heating technique.

A new pyrometer which detects radiation in a band from 1.1 eV to 1.3 eV was therefore purchased. Between room temperature and ~ 400°C, the bandgap of GaAs is above 1.3 eV and therefore the pyrometer will sense the heater filament temperature of 1000°C and will not be effective in controlling the substrate temperature. However, as the substrate heats its bandgap shrinks to < 1.3 eV for temperatures > 400°C and the pyrometer then measures the temperature of the GaAs. Also, as the substrate temperature increases and the bandgap of GaAs shrinks, the heater energy is more efficiently coupled into the substrate. At temperatures above 400°C the substrate temperature is directly controlled by the power input into the heater filaments. Thus we have achieved both effective and

efficient substrate heating and accurate temperature sensing.

However, even after these changes, a small, but significant temperature nonuniformity was observed across the wafer due to the nonuniform location of heaters and the presence of the thermocouple and the auxiliary shielding in the heating station. A PBN/PG/PBN backing plate was therefore placed between the substrate and the heating filaments for efficient lateral dispersion and transfer of heat into the GaAs substrate. The thin layer of PG (0.075 mm) was sandwiched between two protective layers of PBN to enhance conductivity. This scheme has been shown to provide very uniform heating but it is difficult to heat the substrate above 650°C. We are, therefore, currently reducing the diffuser plate thickness to achieve more efficient heating of the substrate while maintaining efficient lateral heat dispersion and are also considering using a sapphire heat diffuser in place of the PG/PBN to see if it has better properties.

We are currently characterizing the lateral uniformity and quality of the epitaxial layers produced using these growth techniques by measuring the photoluminescence properties of various quantum well structures across a 2" wafer. These measurements should provide a sensitive test of material composition, thickness and quality. Thus, we soon expect to have these problems successfully resolved.

4.0 References

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